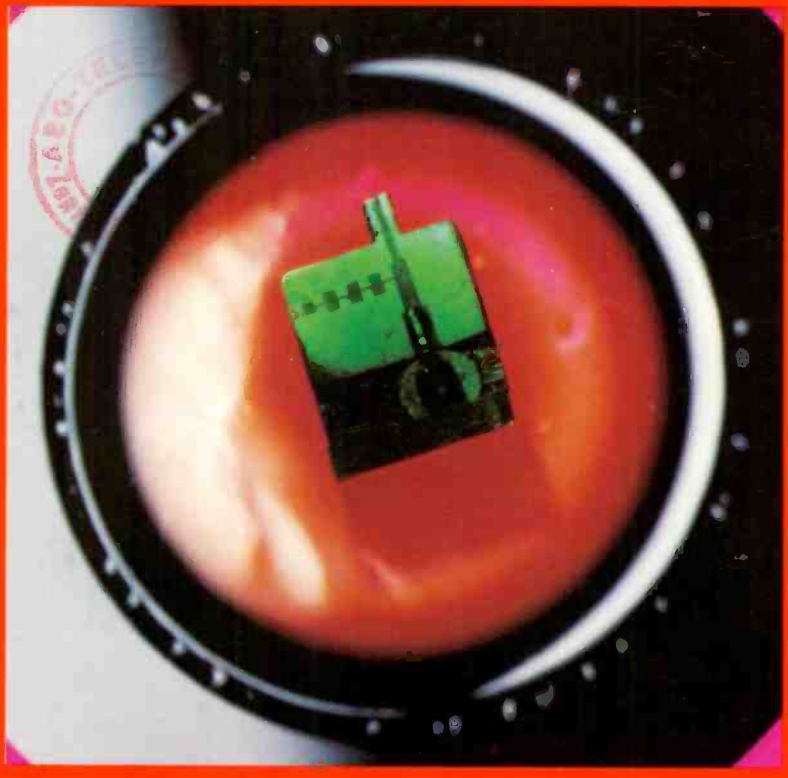
RCA Review



Si Millimeter-Wave IC Seen Through Si Wafer

December 1984 Volume 45 No. 4

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Our cover shows a Silicon Millimeter-Wave Integrated Circuit (SIMMWIC) seen through a 1–2 μm thick Si wafer similar to that used to make the IC. The SIMMWIC technology, which includes high-energy ion implantation, pulsed laser annealing, and novel wafer thinning, is described in the paper by Stabile and Rosen in this issue of *RCA Review*.

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Contents

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Introduction to Special Issue on Microwave Devices and Circuits

In this special issue of *RCA Review* the reader will find some of the papers presented at the IEEE Princeton Section Sarnoff Symposium on Microwave and Millimeter-wave Devices and Circuits held at RCA Laboratories on March 24, 1984. This annual Symposium is gaining popularity among researchers, both in the government and in industry, working in the area of advanced microwave technology, and has spurred the publication of special issues of the *RCA Review* devoted to the microwave art.

Reflecting current interest in the field, several of the papers describe advances in the practical utilization of millimeter-wave circuits and devices. Applications of power sources for millimeter-wave systems (Thoren) and the design of passive monolithic components (Binari et al.) are discussed, as is a new look at high-resistivity silicon for the construction of monolithic millimeter-wave circuits (Stabile and Rosen). R. Camisa et al. present an approach to monolithic circuits in gallium arsenide in which the usual tradeoff between thermal and electrical properties of the circuits is circumvented. The remaining papers are devoted to components specifically designed for satellite communications systems, another area where the microwave technology has been preeminent: communications receivers (Goldberg and Dhillon), driver amplifiers (Moochalla and Aubert), and power amplifiers (Dornan et al.) all use state-of-the-art GaAs FETs and hybrid circuit techniques.

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Advanced Applications and Solid-State Power Sources for Millimeter-Wave Systems*

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Abstract—Millimeter-Wave technology offers many advantages for communications and missile systems of the future. These benefits are presented with a discussion of their impact on millimeter-wave systems under development, including smart munitions, minimissiles, communications, fire control, and radiometry. Millimeter-wave solid-state power sources, in particular the IMPATT diode, have made lightweight integrated high-frequency systems a reality. The development of these power sources, including IMPATT power combining, is presented.

1. Introduction

Millimeter-wave technology has emerged from the laboratory into the forefront of systems development for the 1980s. Millimeter-wave frequencies were usually relegated to custom applications and prototype systems, principally for the military. That has changed. The military is now committed to use of millimeter waves in programs such as MILSTAR (Military Strategic Tactical and Relay) and MLRS (Multiple Launch Rocket System).[1,2] Lockheed is funded to develop the MILSTAR satellite network. It has been estimated that the component market for MILSTAR terminals alone could reach millions of dollars per year by 1990. MLRS will initiate a multiyear, multinational development program with many millions to be com-

* Part of this paper is a revised version of a paper published in the *Microwave Systems News* (*MSN*) in September 1983, p. 109. This paper was presented at an IEEE Princeton Section symposium on "Microwave and Millimeter-Wave Solid-State Devices and Circuits" held at RCA Laboratories, Princeton, NJ on March 24, 1984.

mitted to developing an autonomous minimissile, called the "terminally guided submunition", containing its own active millimeter-wave seeker. Commercial applications for secure communications links and satellite-to-satellite data links are also emerging. These commitments by government and industry have initiated a new era in the development of millimeter-wave systems. One of the prime technological thresholds crossed in reaching this new status was the advent of the solid-state transmitter using Gunn diodes, IMPATT diodes, or both.

In this paper we first discuss the status of millimeter-wave system development and then describe solid-state power sources for use with these systems.

2. Advantages of Millimeter Waves

Millimeter waves offer many advantages over microwave or infrared systems. A few key features are:

- Lightweight
- Small Size
- Broad Bandwidths (several GHz)
- Operation in Adverse Weather (cuts through fog, haze, smoke, dust, and debris)
- Narrow Beamwidths with High Resolution, Resistance to Jamming, and Low Probability of Intercept
- Covert Capability of 60 GHz
- May "See" Stealthy Targets (absorbers at 10 GHz reflect at 100 GHz)

These features are exploited in a large array of systems applications beside the MILSTAR and MLRS program, e.g., radio Astronomy has been using higher frequency equipment for many years. Other special applications include clear-air turbulence detectors, weather radars, nuclear spectroscopy, missile guidance, fuzes, motion detectors, map-matching radars, plume detection, and air-traffic-control beacons. However, the use of millimeter waves in systems that required large production runs awaited the arrival of a solid-state power source and a more mature component technology for all the high-frequency parts. The inherent advantages of small size, high reliability, and lightweight could only be realized in the total system when the millimeter-wave power source was also small, low voltage, reliable, and obviously lightweight. With the development of the IMPATT diode, made from silicon or gallium arsenide, and the Gunn diode, made from gallium arsenide or indium phosphide, suitable power sources became available with a

sufficiently high confidence level to permit the development of major systems.

Of equal importance in the quest for millimeter-wave capability is an understanding of the device physics and the availability of instrumentation to measure and evaluate the various system components. An example is the wealth of information that can be obtained from an automatic network analyzer at millimeter-wave frequencies. As circuits get smaller (proportional to the smaller wavelengths), it becomes more difficult to predict their behavior based on simple circuit models. Diode packages and even imprecise machining of the component housing can yield large reactive and resistive parasitics that drastically affect the performance of a component. Clever use of the network analyzer can isolate these problems, aid in circuit design for broadband performance, and confirm theoretical predictions of solid-state physics for power sources such as the IMPATT diodes.

Only very recently has capable instrumentation become available to exploit accurate component design techniques. It is difficult to envision large production runs of millimeter-wave components without first understanding the physics of the design and carefully accumulating the measurement data to validate the circuit design. The device physics, most notably for GaAs IMPATTS above 40 GHz, have only recently been explained. Above 100 GHz, the instrumentation for accurate network analysis is not available.

3. The Millimeter-Wave Spectrum

Millimeter-wave frequencies span 30 to 300 GHz where the wavelengths range from less than one centimeter to more than one tenth of a centimeter. The principal frequencies of current interest are centered around 35, 44, 60, 94, 140, and 220 GHz. The reason is simple. Fig. 1 shows the average atmospheric absorption of millimeter waves for horizontal propagation. The features are quite distinctive. Atmospheric "windows" where absorption reaches a local minimum are found at about 35, 94, 140, and 220 GHz. An interesting O_2 absorption peak occurs at 60 GHz and can be exploited for secure communications. MILSTAR uses 44 GHz as an uplink to the satellite system and 20 GHz as a downlink. 44 GHz was chosen in part for its ability to sustain a broad bandwidth, its inherently jam-resistant narrow beamwidth, and its "small size" componentry. At 44 GHz, the atmosphere still has favorable propagation characteristics.

The maturity of the components decreases as the frequency in-

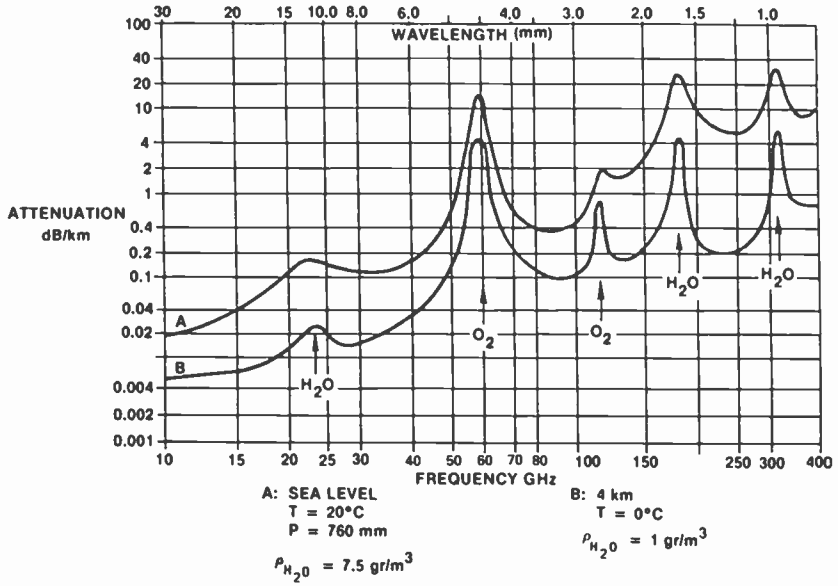


Fig. 1—Average atmospheric absorption of millimeter waves.

creases. Below 50 GHz, the components and measurement techniques are proven and large production capacity can probably be reached with confidence. At 60 GHz and above (especially at 93–95 GHz), the components are less mature, but are available and are being vigorously developed (see Fig. 2). A concerted effort by industry, with backing by the government through such programs as MLRS and MILSTAR, should bring production capability along at a rapid pace.

4. Future Systems

Table 1 lists over sixty applications of millimeter-wave systems. This table is from a new text, "Millimeter Wave Engineering and Applications", by Bhartia and Bahl published by John Wiley and Sons (1984).[3] It is a good reference for those embarking on millimeter-wave technology and component design.

I've chosen to isolate a few key applications that are probably the focus of the government and industry investment in millimeter waves. These systems are discussed below. By exploring some of the characteristics of each of these system applications, with examples

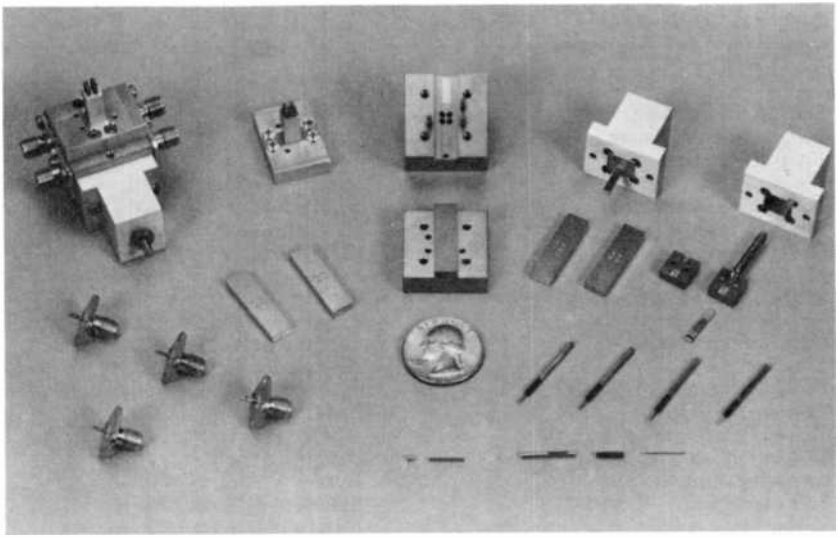


Fig. 2—94-GHz IMPATT diode power combiner. Assembled unit is shown at upper left in photo.

that are available, we can gain an appreciation for the challenge of millimeter-wave systems.

Smart Bullets

A smart bullet is distinguished from a minimissile because it is launched from a gun. The terrific impulse generated by the ignition of the charge in the gun barrel imparts between five and fifteen thousand or more *g*'s to the projectile. The smart bullet carries with it either a millimeter-wave transceiver (a radar), a forward-looking receiver to detect a target that someone is illuminating with a millimeter wave transmitter, or a rearward-looking receiver to get command guidance information. One possible projectile for such a smart bullet application is the Copperhead 155mm projectile. Currently the Copperhead detects the reflection of a laser that is pointed at the target while the projectile is in flight. The same designation technique could be achieved with a millimeter-wave, hand-held illuminator.

A smart bullet is maneuvered by popout fins or small explosive charges that impart a lateral force to change the trajectory. It usually does not carry a rocket motor for extended ranges.

Smart bullets offer the expected advantage of a high probability of hitting the target on each shot. It has been estimated that 100

Table 1—Millimeter-Wave Applications

Radar	
Low angle tracking	Remote sensing of the environment
Secure military radar	Surveillance
Interference free radar	Target acquisition
Cloud sensing radar	Missile guidance
High resolution radar	Navigation
Imaging radar	Obstacle detection
Ground mapping	Clutter suppression
Map matching	Fuses
Space object identification	Harbor surveillance radar
Lunar radar astronomy	Airport surface detection radar
Target characteristics	Landing aids
Weather radar	Air traffic control beacons
Clear-air turbulence sensor	Jet engine exhaust and cannon blast
Target designators	Beam riders
Range finders	Passive seekers
Detection/classification of ground vehicles	Imaging
LPI radar	Hand-held radar
Radar cross-section measurements	Active missile seekers (terminal guidance)
Communications	
Secure military communications	Satellite to satellite communications
Point to point extremely wideband communications	Inter satellite relays
Spacecraft communications during blackout	Earth to space communications
Interference free communications	Retroreflector communications
	LPJ communications
	Railroad communications
Radiometry	
Remote sensing of the environment	Ground target detection
Radio astronomy	Missile detection
Radio sextant	Missile guidance
Ship detection	Clear-air turbulence sensor
Space-based radiometers	
Instrumentation	
Plasma diagnostics	Automatic braking
Rocket exhaust plume measurements	Spectroscopy
Remote vibration sensor	Prediction of blast focusing
Model radar cross-section measurements	Classroom demonstration of optics

to 200 randomly placed "dumb" rounds bombarding a target area are needed before one effectively hits a target. The logistics of carrying that many shells imposes a serious burden on front line forces. The smart bullet offers an effective alternative.

Minimissiles and Missiles

A more sophisticated approach to the intelligent munition is the minimissile. Hughes Aircraft has conducted extensive tests on a

millimeter-wave minimissile developed for the Air Force called WASP (wide-area smart projectile). The feasibility of such a missile with a pulsed 94-GHz active seeker radar has been proven. Targets were acquired and a tank was hit as the WASP glided in on the returning radar signature. The WASP missile was intended for a multimissile pod dispenser placed under the wing of an aircraft. Unfortunately the cost per round of this advanced system was too high and development was concluded.

The Army is sponsoring an exciting new program called MLRS in cooperation with development partners Great Britain, France, Italy, and the Netherlands. The Multiple Launch Rocket System (MLRS) is a tracked vehicle that contains two "six packs" of missile launchers (12 missiles overall). To make these battlefield missiles more effective, six new millimeter-wave minimissiles will be contained within each main missile. At a predetermined time, each main missile will eject the six terminally guided submissiles (TGSM's) which will glide over the target area and look down with their millimeter-wave radar for targets. Each minimissile has a high probability of finding a target in a "target-rich" environment and will swoop in for a near-vertical hit on the less armored topside of the tank. Sophisticated signal processing will eventually enable the missile to categorize and classify each target by its radar return as a tank, truck, or artillery piece.

Modifications of such minimissiles can be envisioned for air-to-air, air-to-ground, and ground-to-air applications as well. The ability to see stealthy targets may be an advantage for millimeter-wave minimissiles. Absorbers at X-band are often highly reflective at W-band. "Smooth" contours at lower frequencies can look more pronounced at W-band as the radar resolution increases. So missiles used against low-cross-section cruise missiles or stealth-like aircraft may be suitable for millimeter waves. Because of the economy of size and weight in high-frequency systems, a dual-mode IR/MMW or 35-GHz/94-GHz radar can be considered. Each of these dual-mode approaches exploits the ability of millimeter-wave radar to see through fog, dust, clouds, smoke, and debris, environments in which infrared and optical guidance systems will not operate.

As mentioned earlier millimeter-wave radars are also hard to jam. First you have to find the missile, and then you need to point the jammer at the missile. This also assumes each target has the state-of-the-art componentry required to constitute a millimeter-wave jammer. Fig. 3 illustrates the narrow beam projected at millimeter-wave frequencies; 94-GHz beams can be two degrees or less in beamwidth.

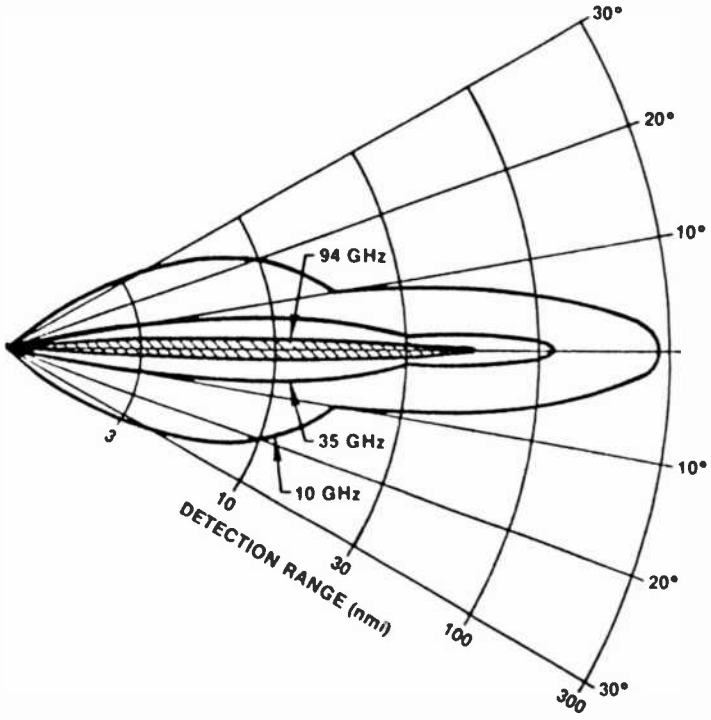


Fig. 3—94-GHz "pencil-beam" antenna pattern. Obviously, such a narrow beam is highly jam resistant.

Another interesting dual-mode system for minimissiles combines the successful anti-radiation homing capabilities, already developed, with a terminal guidance millimeter-wave radar. In the event that the radar station being homed on turns off, the millimeter radar on the missile turns on and searches the limited area that the missile is heading for to acquire the target. All these applications fall under the category of "fire and forget".

A new arena for millimeter-wave radar and millimeter-wave guidance systems is space. The newly formed Strategic Defense Initiative is a research and development program to evaluate the technology available to provide a robust defense against tactical and strategic ballistic missiles for the United States and NATO. Surveillance radars, space-based kinetic energy weapons (missiles), fire-control radars, and surface-launched missiles are potential candidates for millimeter-wave approaches. Proof of principle and trade-off studies are underway to assess the capability of various approaches to each of these systems. The high resolution offered by

millimeter-wave systems, even at ranges of a thousand kilometers or more, may provide significant advantages, especially in isolating real targets from decoys.

Communications

Taking advantage of the lighter weight, broad-bandwidth capability, small size, and especially the low probability of intercept, satellite communications networks have become a dynamic market for millimeter-waves. Uplinks at 30 and 44 GHz are being made for commercial and MILSTAR applications.

Downlinks at 20 GHz are also being developed for these systems. Satellite crosslinks for secure communications are being developed at 60 GHz. The high absorption peak at 60 GHz makes either jamming or eavesdropping from the ground virtually impossible. The narrow beamwidths also assure communication links that can't be easily intercepted even in space. Very high data rates can be transmitted over channels with more than a couple of GHz of bandwidth. Also, many channels can be provided.

A close look at the scope of the MILSTAR program will provide a sense of the commitment and the development effort that is spurring a large investment in millimeter-wave development by industry.

MILSTAR is scheduled to be in place as a nuclear survivable communications network in the 1990's. There will be four satellites in geosynchronous orbit with three more in polar orbits. It is expected that more than 4,000 strategic and tactical MILSTAR terminals will be placed on ships, aircraft, ground equipment, and submarines. The Army, Navy, and Air Force are each supporting program development efforts. The overall system integration is being run by the Air Force Space Division.

In 1986–87 the Navy program NESP (Navy EHF Satellite Program) will test six EHF terminals. Three will be ship mounted, two on submarines, and one land based. An attachment (called an EHF applique) to the FLTSATCOM satellite will be the spaceborne link. Raytheon and Harris are funded to develop these terminals for delivery in 1986. Both companies have shown substantial progress. Raytheon is developing solid state transmitters and a TWTA capable of more than 200 watts. Typical NESP antennas being developed by Harris include a 2-ft shipboard dish, a 5-ft ground based dish, and a 3-inch periscope-mounted design. The Navy is seeking 400 MILSTAR terminals in their initial acquisition.

The Air Force Electronic Systems Division has contracted with

two teams to develop terminals for B52's, B1B's, E3A's AWACS, and E4 aircraft. The teams of Raytheon/Rockwell and Hughes/MA-COM each have $40 million to develop the prototype airborne terminals in the first phase of this development. The second phase winner will be required to build 20 to 25 terminals over two years for about $200 million. Advanced technologies such as VHSIC and GaAs monolithic microwave modules will likely be used in this effort especially for the 20-GHz receive array. Monolithic GaAs circuits above 30 GHz are at the cutting edge of the state of the art and require further development.

The space segment under the supervision of Lockheed will of course need 44-GHz receiving networks. Hughes Space and Communications Group is supplying the EHF component expertise for the 44-GHz receive and 20-GHz transmit portions of the satellite.

As can been seen, the depth and breadth of the MILSTAR program represents a serious and exciting business opportunity and the major motivation for rapid development of 44-GHz technology and systems.

On the ground (within the atmosphere), 60 GHz offers a unique approach to secure communications. Since 60 GHz is rapidly attenuated by the O_2 absorption in the atmosphere, the antenna sidelobes of a "secure" link are nearly impossible to pick up. If the transmitter and receiver are tuned for optimum performance in the secure mode (i.e., receiver at maximum sensitivity with transmitter at minimum necessary power levels), then any receiver (or detector) that might be present beyond the line-of-sight receiving station will have a difficult time receiving the signal. The narrow beamwidths add even greater resistance to interception to this secure, station-to-station system.

Fire Control

Millimeter-wave systems are exceedingly well suited for fire control. It may be difficult, however, to scan the entire sky with the narrow millimeter-wave beams, though there are some "fan beam" designs that can accomplish this. Let us assume that a smaller search volume has been isolated by IR or lower-frequency radar. Now the beamwidths of millimeter-wave radars can be used to decided advantage. The Advanced Fire Control Radar (AFCORS) program at Raytheon showed that the narrow beamwidths at W-band could lock-on and track an aircraft target right down to the treetops. The low altitude clutter environment had little or no effect on the radar; conversely, X-band and Ka-band radars may have difficulty

in holding track on the control of low flying targets. Fig. 4 depicts the portion of the beam that would interact with the ground for Ka-band (16 GHz) and for 94 GHz. Clearly the lower frequency might be susceptible to "terrain-bounce" effects, resulting in a false "virtual" image that appears to be below the ground. So anti-aircraft-gun pointing radars could realize an advantage by using millimeter-wave. The Army's Surveillance and Target Acquisition Radar for Tank Locator and Engagement (STARTLE) system was designed to locate opposing tank forces in fog, smoke, dust, etc., and to provide fire control information such as range and direction. One approach for this radar operates at 94 GHz. The published STARTLE system parameters are:[4]

Frequency: 94 GHz
Beamwidth: 11 milliradians
Average Power: 0.1 to 0.5 watts
Antenna Aperture: 14 inches
Field of View: 15 degrees × 7.5 degrees wide
5 degrees × 2.5 degrees narrow
Target Detection: 3000 meters
Target Tracking: 15 mrad @ 2 km

Millimeter-wave fire control radar may be modified to be carried on aircraft such as helicopters or close-support jets. A target acquisition radar might use a millimeter-wave illuminator to "paint" the

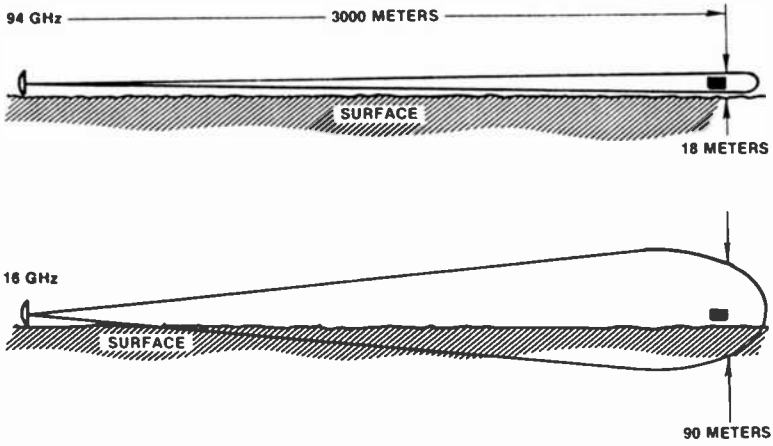


Fig. 4—Low-level detection radar beams for 94 GHz and 16 GHz. As can be seen, for low-angle application, lower frequencies direct a major fraction of energy into ground resulting in a multipath interference pattern that compromises the integrity of the beam.

target with millimeter-wave signal, while a precision guided munition is launched or a semismart cannon shell is fired from the aircraft.

One interesting aspect of the fire control mission is the challenge of seeing and engaging the possible "stealth" targets of the future. There are well known techniques for lowering the radar cross section of targets, including the use of microwave absorbing coatings and the designing of smooth contoured surfaces that scatter the incident microwave radiation instead of reflecting it back to the tracking antenna. Millimeter-wave systems offer a means of countering these techniques. Materials that absorb energy well at X-band become much more "reactive" at W-band and hence reflect the millimeter-wave signals. A multilayered coating that is a good attenuator over a decade of frequencies might extract a formidable weight penalty on the aircraft.

Similarly, smooth surfaces at X-band might yield larger returned signals when the higher resolution millimeter-wave system is employed. Thus, there is an inherent anti-stealth capability in millimeter-wave tracking and fire-control systems.

Radiometry

An overview of radiometry will round off this brief excursion into the emerging challenges of millimeter-wave systems.[10]

A radiometer is basically a very sensitive and quiet (low-noise) receiver used to detect the "radiometric temperature" of objects, atmospheric effects, and targets. The contrast between the black body emissivity of the ground and the excellent reflectivity of a metal surface (emissivity $\cong$ zero) of a metal target such as a tank make radiometric imaging possible. The ground temperature is usually near 290 K, while the sky temperature that would be reflected by a metal object is much lower. The radiometer detects the temperature contrast. The temperature of the sky will of course change with the weather, making detection more difficult in adverse weather for such a "passive" radiometric system.

An alternative to passive radiometry is "active" radiometry where a noise source or millimeter-wave illuminator is beamed at the target. The target then becomes "hotter" than the background temperature and a detector can see it. Millimeter-wave radiometers would tend toward higher frequencies of 140 GHz and 220 GHz if the target of interest was smaller than the beamwidth being observed. This is determined by a beam filling factor (BFF) which is simply

$$\text{BFF} = \frac{\text{Projected Target Area}}{\text{Projected Beam Area}}$$

The narrower beamwidths of higher frequency systems will of course have higher resolution capability to counter this problem. It is also possible to use active radiometry to increase the range of detection of the target and then switch to passive radiometric tracking when the receiver is near enough to the target so that the temperature contrast can be used for "covert" (listening only) terminal guidance.

The challenge of millimeter-wave systems and technology development is one of the premier arenas for creative and aggressive engineering. The brief overview presented here barely scratches the surface of a tremendous variety of component development efforts.

5. Millimeter-Wave IMPATT Technology

One of the key technological breakthroughs mentioned earlier is the advent of solid-state power sources that allow the fully active millimeter-wave system to realize the low-voltage, lightweight, small radars and communications networks that were envisioned decades ago. Among these are Gunn diode oscillators, pulse-generating exciters with varactor multipliers that may include high frequency surface-acoustic-wave (SAW) devices; new low-loss, high isolation circulator and isolator assemblies; integrated hybrid receivers (and soon monolithic receivers); and IMPATT diode transmitters. Unfortunately, the capability of three-terminal FETs for producing substantial power rapidly deteriorates above 30 GHz, since the dimensions of the gate electrode become much less than a micron. Production yield also decreases as the fabrication technology for FETs becomes more exotic and the ability to generate ample power drops. So, the preferred and only currently acceptable source of power for millimeter-wave systems that are lightweight, portable, and operate with low voltages, are IMPATT diodes.

A survey of the current status of millimeter-wave IMPATT diode technology must cover three important areas:

- IMPATT diodes (silicon, GaAs, and InP)
- IMPATT diode power combiners
- What next for higher power?

5.1 IMPATT Diodes—Silicon, GaAs, and InP

Silicon IMPATT diodes have led the way to higher power and higher millimeter-wave frequency operation. These silicon devices have

been incorporated into systems up to more than 200 GHz. They are currently available as commercial products from Hughes up to 170 GHz, but the cost per diode at these very high frequencies is substantial.

The silicon IMPATT is generally a double-drift structure grown by vapor-phase epitaxy in which both electrons and holes drift as charge packets to contribute to the generation of millimeter-wave power. The efficiency of silicon diodes, like that of any IMPATT, drops off with increased frequency as shown in Table 2. A comparison of the best results and typical performance of current silicon, GaAs, and InP IMPATTs is also shown there. Hughes, TRW, RCA, and Martin Marietta are proceeding with the development of silicon IMPATTs.

More recent research and development of GaAs and InP IMPATTs has led to performances that challenge the role of silicon IMPATTs (Fig. 5). The potentially higher efficiency of both GaAs and InP may lead to their preferred use as power sources in solid-state transmitters. Until recently, GaAs IMPATTs were thought to be limited to frequencies below 30 GHz because of the large intrinsic response time of electrons and, hence, a very slow avalanche process. This is not the case. GaAs has surpassed silicon in performance at frequencies up to 30 GHz by providing more CW power with higher efficiency and equivalent pulsed power performance.[6] Near 40 GHz, GaAs IMPATTs have produced more than 2.5 W of CW power and delivered efficiencies exceeding 21.5% (Fig. 5). Work is underway at Raytheon, Hughes, and TRW to improve the performance of GaAs at higher frequencies (Fig. 6).

New techniques of material growth and doping such as ion beam implantation and molecular beam epitaxy are being used to define the precise mesa structure of these diodes. Millimeter-wave IMPATTs can be considered a "vertical" submicron device because of the very small dimension of the active regions that must be precisely defined and built. Each drift zone of a 40-GHz GaAs IMPATT is less than one half micron for a hard punch-through diode. Because of the exceedingly short drift zones, a closer look at the device physics involved in producing oscillations in GaAs IMPATTs has led to a new model of IMPATT operation, the "delayed secondary avalanche mode."[7,8] Slower than expected electron velocities and constant avalanching throughout the IMPATT demand accurate design dimensions for the phasing of hole and electron "waves" in order for the IMPATT to operate at millimeter-wave frequencies. This delayed-secondary-avalanche mode (DSA mode) will be confirmed

Table 2—Millimeter-Wave IMPATT Performance (30–300 GHz)

Frequency (GHz)	CW		Pulsed	
	Single Diode	Power Combined	Single Diode	Power Combined
30		10W 8-Diodes		
35	1.5W[A] η = 15% Typical	5W 8-Diodes	28W_{pk} MAX[E] 12–17W_{pk} Typical 9.3W_{pk} (32GHz)[F]	
40	2.5W MAX[A] $\eta \leq$ 21.5% 2.0W (InP)[G] η = 8%	11W[B] 12-Diodes (41 GHz)		
60	1.6W MAX[C] 0.8–1.0W Typical[D]	2W[H] 4-Diodes		
94	0.9W MAX[I] η = 5%	1.89W[J] (CW-like p.w. 10 μs at 50% D.C.)	15W_{pk}[E] η = 7% D.C. = 5% 5–10W_{pk} Typical	63W_{pk}[K] (92.5 GHz)
140	0.50 mW[I] $\eta \cong$ 2%		5.6W_{pk}[E] MAX 3W_{pk}[E] Typical	9.2W[E] 4-Diode 5.2W_{pk}[E] 2-Diode
220	50 mW[I] MAX η < 1%		1.0W_{pk}[E] MAX 0.7W_{pk}[E] Typical	1.05W_{pk}[E] 2-Diode (216 GHz)
240	50 mW MAX 25 mW[I]		0.62 W_{pk}[E] MAX	

Millimeter-Wave IMPATT Performance Key

A. Raytheon GaAs Hybrid Profile Double Drift
B. TRW with Hughes Silicon Diodes
C. Hughes T_j = 330° η = 7%
D. T_j = 250°C η = 5–6%
E. Hughes Pulsed Silicon Double Drift Pulsewidths 100–200 ns max Duty Cycle (D.C.) <2% max
F. TRW Indium Phosphide Single Drift η = 10.6% 500 ns Pulsewidths 1% Duty Cycle
G. TRW Single Drift InP IMPATTs
H. TRW with Hughes Silicon
I. Hughes Silicon Double Drift Flat Profile CW Diodes
J. Raytheon 4-Diode Combiner with Commercial Hughes Silicon IMPATTs
K. Hughes Four 2-Diode Kurokawa Waveguide Combiners with Hybrid Waveguide Coupler (8-diodes total) D.C. <2% Pulsewidths <100 ns

as GaAs IMPATTs perform at higher and higher millimeter-wave frequencies.

InP IMPATTs are under development at TRW and have shown very promising initial results at the lower millimeter-wave fre-

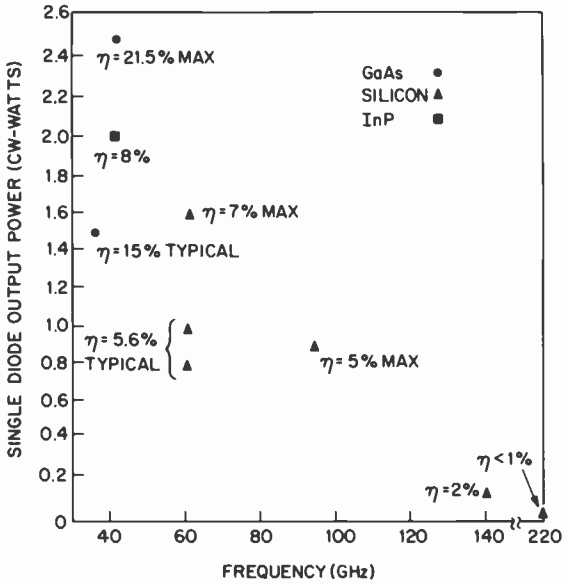


Fig. 5—Single-diode output power versus frequency for recently developed GaAs, Si, and InP IMPATTs indicating the efficiency of the devices. Higher efficiency of the GaAs and InP devices may lead to their preferred use as power sources in solid-state millimeter-wave transmitters.

quencies. InP material fabrication techniques are not as mature as either those of GaAs or silicon, even though material growth and metallic contact techniques of both these latter materials are still evolving. As the fabrication technology advances, TRW expects improved results from InP IMPATTs. Currently, performance ranges from 9.3 W_{PK} at 32 GHz with 10.6% efficiency to about 2.5 W_{PK} at 40 GHz and 5.7% efficiency.[9] These results have been achieved for 500-ns pulses at 1% duty cycle. Ultimately more than 15% efficiency at 60 GHz is expected from properly designed InP IMPATTs.

5.2 IMPATT Diode Power Combiners

As the performance of the individual device is constantly improved through more accurate fabrication techniques, so too are the circuits in which the diodes must operate. The desire for still higher levels of power is satisfied by combining the power of many IMPATTs in a power combiner circuit. At lower frequencies (typically less than 20 GHz), there are many alternatives for power combining IMPATTs.[6] Above 30 GHz, however, the physical size of the millimeter-wave power combiner rapidly decreases as the frequency increases.

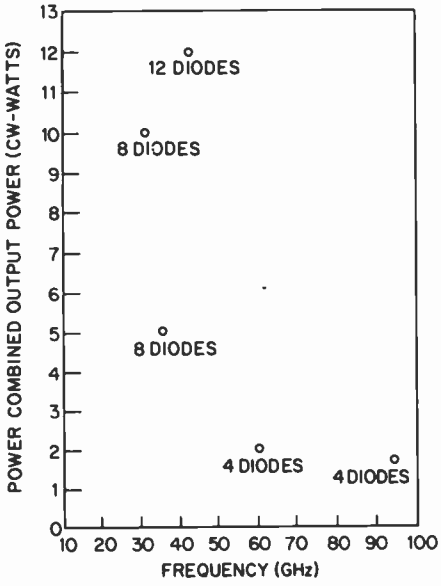
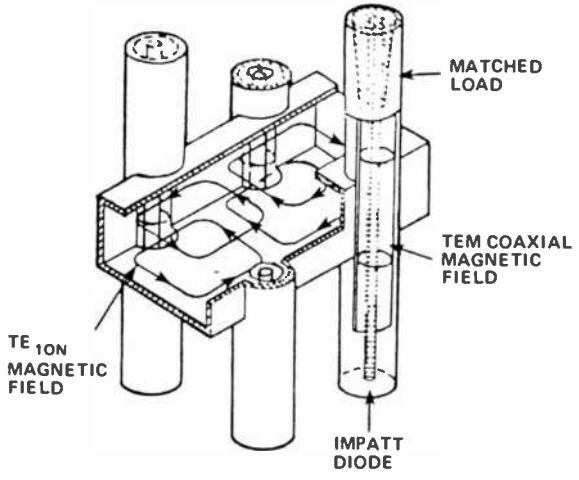


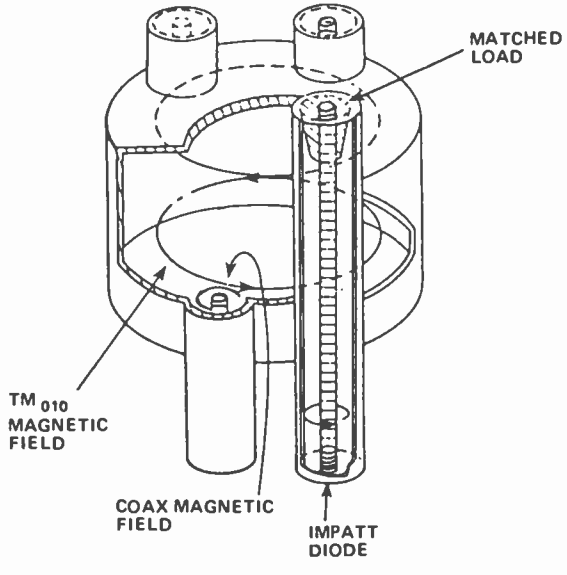
Fig. 6—Higher levels of power are achieved by combining the power of several IMPATTs in power combiner circuits, particularly above 30 GHz.

The preferred technique for power combining IMPATTs at 10 GHz is the circular cylindrical cavity in which the diodes are arrayed around the periphery of the cavity as tightly spaced as possible. Fifteen to eighteen diodes may fit around a fundamental TM_{010} mode cavity, while more than twice that number can surround a TM_{020} higher-order mode cavity at 10 GHz. At 35 GHz, however, the diameter of a TM_{010} mode cavity limits the number of IMPATTs to only a few. A TM_{020} cavity of larger diameter might allow an array of 12 to 20 diodes but requires additional mode dispersion techniques to make certain that the diodes oscillate at only the desired frequency. These tightly packed circular cylindrical cavities are not very useful above 45 GHz and are replaced by a Kurokawa waveguide combiner (Fig. 7) as the preferred IMPATT combiner circuit. The size of the diode package, which may be only 50 mils in diameter, becomes a significant fraction of a wavelength at millimeter-wave frequencies. At 100 GHz, the size of a full-height waveguide is 100 mils across and 50 mils high.

In the Kurokawa waveguide combiner the diodes are arrayed on both sides of the waveguide and spaced at $\lambda_g/2$ (λ_g = waveguide wavelength) so that their output power can be added constructively in the standing wave that is set up by the resonance of the cavity.



TE_{10N} RECTANGULAR WAVEGUIDE CAVITY COMBINER



CIRCULAR CYLINDRICAL TM_{010} CAVITY COMBINER

Fig. 7—Tightly packed circular cylindrical cavities are replaced above 45 GHz by a Kurokawa waveguide combiner as the preferred combiner circuit.

TRW has reported 11 W_{cw} with 12 silicon IMPATTs at 41 GHz in such a Kurokawa waveguide combiner, and at about 60 GHz a four-diode combiner provided about 2 W_{cw} from silicon IMPATTs (see Fig. 6). Two notable results were reported for W-band Kurokawa waveguide power combiners. Hughes achieved 63 W_{pk} from four two-diode waveguide combiners in a network of hybrid waveguide couplers.[11,12] This result was for low-duty-cycle operation (<1 percent) and pulsewidth of 50 to 100 ns. Raytheon recently reported 1.89 W_{pk} from a four-diode power combiner at duty cycles from five to 35% and easily tunable from 90 to 99 GHz.[13] The long pulsewidth and high-duty-cycle operation approached CW-like operation. A newly designed precision tuning element was used to facilitate the rapid tuning of the silicon IMPATTs used in the combiner. At 140 GHz, an experimental four-diode combiner has achieved 9.2 W_{pk} and an experimental two-diode Hughes combiner has achieved 5.2 W_{pk} at low duty cycles and short pulsewidths.

As a more detailed understanding of the interaction of the IMPATT and the power combiner circuit is established, higher performance circuits with improved combining efficiency and broader bandwidth performance will be achieved. One of the limiting factors of IMPATT performance is the physical package in which the diode is mounted. The package acts like a resonant circuit so that the parasitic inductance of the IMPATT beam leads or bonding wires and the parasitic capacitance of the quartz or ceramic ring limit the bandwidth of the diodes' operation. Simulations of the device physics of IMPATT diodes show that it is inherently a broadband device. At 20 GHz and 40 GHz, bandwidths in excess of 20% and 10%, respectively, have been achieved in custom-designed single-diode amplifier circuits. As the desired frequency increases and the package becomes a substantial fraction of a wavelength, the detrimental bandwidth-limiting parasitics are a serious concern. Additional research and development of low parasitic packages will be valuable.

6. What Next for Higher Power?

As the development of better and higher performance IMPATTs progresses, an assessment of the potential capabilities is important. What material growth techniques are the most promising? What are the expected physical limitations?

Ion-beam implantation of selected dopants is a very effective way of achieving highly doped layers. The InP diodes discussed above are fabricated by ion implantation. This process, however, usually

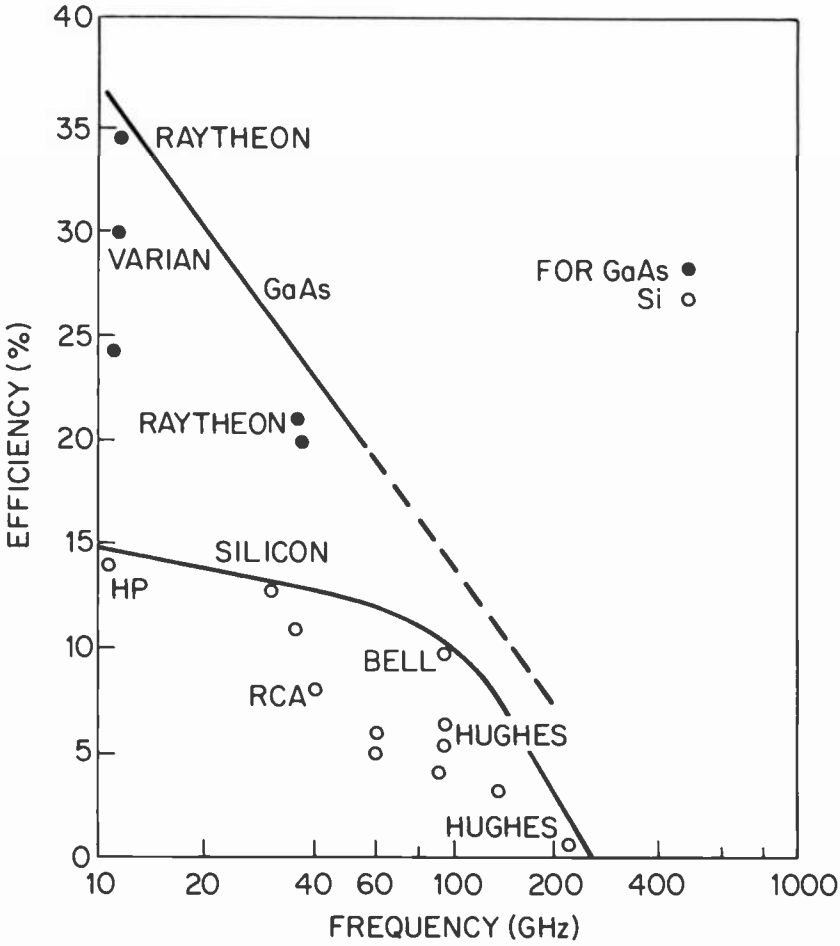


Fig. 8—GaAs has surpassed Si in performance at frequencies up to 30 GHz by providing more CW power at higher efficiencies. Near 40 GHz, GaAs IMPATTs have delivered efficiencies exceeding 21.5%. Work is currently underway at Raytheon, Hughes, and TRW to improve performance of GaAs devices at higher frequencies.

requires an annealing of the substrate to repair the damage caused by the high velocity ions crashing into the substrate. As the substrate is annealed, the doping distribution spreads out and the precise delineation of the doping layers that is needed for accurate IMPATT growth is more difficult to achieve. This is particularly true at higher millimeter-wave frequencies (80 to 110 GHz) where the mesa thickness dimensions are very small. Ions also have a tendency to tunnel between atoms in the substrate crystal lattice and further spread their distribution. This tunneling can be sub-

stantially, but not totally, eliminated by tilting the crystal so that tunneling paths in the lattice are not entered straight on by the ions.

Molecular Beam Epitaxy (MBE) is becoming an important technique for the growth of IMPATT diodes with vertical dimensions having tenths of microns resolution.[14] Bell Laboratories fabricated 10 GHz MBE IMPATTs in 1974.[14] More recently Varian has produced high power X-band IMPATTs and K-band IMPATTs designed for operation above 20 GHz by MBE.[15] The unique characteristics of MBE will make it a viable technique for growing millimeter-wave GaAs IMPATTs in the 50 to 100 GHz range[16] (Fig. 8). Raytheon is currently fabricating GaAs IMPATTs above 60 GHz by MBE.

Molecular beam epitaxy is an ultrahigh vacuum technique for the evaporation of constituent elements of semiconductor compounds. Thin films with controlled dimensions and characteristics are deposited on substrates. GaAs and related III-V compounds are commonly grown in MBE systems.

When GaAs is evaporated, the Ga and As dissociate. So it is very difficult to evaporate GaAs onto GaAs. A method of constructing a GaAs layer is therefore necessary. In MBE, the Ga and As (as well as other elements used to dope the desired film) are thermally evaporated from individual crucibles or cells. These separate cells create molecular beams that impinge on the substrate surface at controlled flux densities based on the evaporation rate due to the temperature of each cell. The recombination of the constituent elements results in a stoichiometric compound, and a layer of desired doping density is achieved. High purity layers can be grown as monolayers (one atom thick). MBE growth allows the abrupt transition of doping levels to be achieved. For millimeter-wave IMPATTs, especially where a Read spike or modified Read structure is desired, the abrupt transition between doping levels would allow very accurate dimensioning of the avalanche and drift zones. The proper phasing of secondary avalanched holes (DSA-holes) in DSA-mode operation depends on such accurate dimensions. The surface quality of MBE films may be superior to that of LPE (liquid-phase epitaxy) or VPE (vapor-phase epitaxy).

Currently a key question that must be answered is whether or not MBE can provide a sufficient quantity of IMPATTs in production. An alternative system of fabrication with higher throughput may be metallo-organic chemical vapor-phase deposition (MOCVD) where the growth process is more like regular chemical vapor-phase growth techniques.

It may be possible to grow heterojunctions or superlattice structures that can tailor the propagation velocity of holes and electrons for still higher performance GaAs IMPATTs up to and beyond 100 GHz. Techniques for growing InP IMPATTs by MBE or MOCVD would provide a very favorable alternative to the less accurate ion-implantation methods.

If accurately doped submicron layers are achieved by MBE for 100 GHz GaAs IMPATTs and the physics of the DSA mode are applied, the predicted performance for such IMPATTs is more than 1 W of CW power at 17 to 20% efficiency. Such a diode would eliminate the need to power combine many diodes of lesser power. High-power modulators used on diodes of considerably lower efficiency (~5% at 94 GHz) would no longer be needed. Additional radar or seeker range could be achieved by power combining this more powerful IMPATT.

The advent and evolution of the IMPATT diode as a millimeter-wave power source has made the possibility of small, lightweight, all weather, reliable, and effective millimeter-wave systems a reality.

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Millimeter-Wave Monolithic Passive Circuit Components

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Abstract—Several mm-wave passive circuit elements have been designed, fabricated, and tested. The circuit elements were designed in a microstrip format and cover the 75- to 150-GHz frequency range. They consist of a terminated 50-Ω transmission line, a Wilkinson splitter, a Lange coupler, and a sum/difference network. The test results on these components demonstrate the feasibility of microstrip circuitry in this region of the mm-wave spectrum.

Introduction

In recent years, there has been considerable interest in the development of millimeter-wave monolithic circuits for potential application in areas such as radar, communication, and wideband electronic warfare. Several mm-wave monolithic circuits have been demonstrated.[1,2] This paper reports on the design, fabrication, and test results of passive microstrip components designed to cover the frequency range of 75 to 150 GHz. These components have been implemented with InP to exploit the potential of InP mm-wave active devices,[3] but the technology is readily transferable to gallium arsenide or silicon.

Circuit Design

The components include a 50-Ω terminated transmission line, a Wilkinson splitter, a Lange coupler, and a sum/difference network. A summary of the circuit design is given here; the details are provided elsewhere.[4] The substrate thickness was chosen to be 50 μm to obtain quasi-TEM operation through 420 GHz and to achieve low-

impedance transmission-line segments. This value of substrate thickness is also the optimum for maximizing the unloaded Q of half-wavelength 50-Ω resonators in the vicinity of 100 GHz.[5] The dielectric constant used in the designs was 12.55. This value of dielectric constant was determined from low- and high-frequency measurements.[4,6] The low-frequency measurements were performed on a metallized rectangular slab of InP. The dielectric constant was determined by measuring the resonate frequencies of the slab from 4 to 18 GHz.[6] This value was confirmed at W-band by modeling the transmission characteristics of linear and ring resonators fabricated on InP.[4]

The passive components are shown in Fig. 1. Each element has 50-Ω input and output transmission lines that extend to the edge of the InP chip. Each chip is 1.6×1.6 mm^2, but in most cases only a small portion of this area contains the passive element. To achieve a transmission-line impedance of 50 Ω on a 50-μm-thick InP substrate, a conductor linewidth of 36 μm was required. The conductor thickness was chosen to be 0.8 μm, which is approximately three skin depths in gold at 100 GHz. The line is terminated with a thin-film 50-Ω resistor that has a length of 18 μm and a width of 36 μm. The resistor is followed by an open-circuited section of 30-Ω transmission line that is one quarter wavelength long at 112 GHz. The Wilkinson splitter[7,8] is shown in Fig. 1(b). It consists of 50-Ω input and output microstrip lines, two uncoupled 14-μm-wide 71-Ω microstrip lines, and a 36×36-μm^2 100-Ω isolation resistor.

The Lange coupler layout is shown in Fig. 1(c). The width of the coupled lines is 1.6 μm, and the separation between lines is 3.0 μm. Four air bridges are used to connect alternate lines. The coupling length is approximately 250 μm. The coupler was designed by use of an in-house synthesis program,[9] and incorporated line-thickness correction in the coupling region.[10] The sum/difference network is shown in Fig. 1(d). It consists of a Lange coupler, a 90° Schiffman[11] phase shifter, and a reference line.

Circuit Fabrication

From a fabrication viewpoint, the circuits can be placed into two categories. The first category, which contains the terminated line and the Wilkinson splitter, required the deposition of relatively large geometry thin-film resistors and transmission-line metallizations. The second category, which contains the Lange coupler and the sum/difference network, required an air-bridge formation in combination with the transmission-line metallization. The second

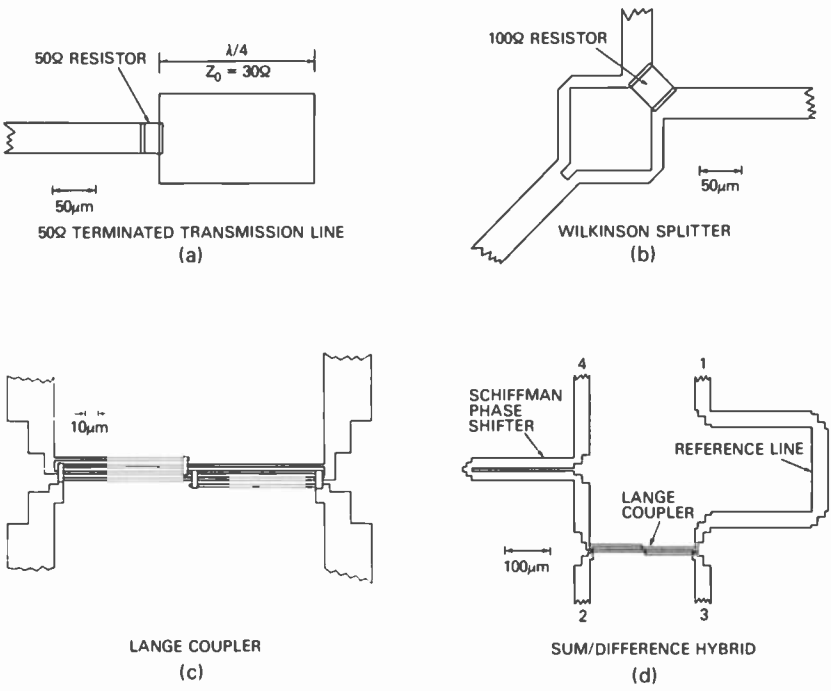

Fig. 1—75- to 150-GHz passive circuit components.

category required much smaller line widths and is considerably more process intensive than the first category.

All of the passive circuits were fabricated on polished, Fe-doped (100), semi-insulating InP. The initial substrate thickness was 400 μm. The resistive material used in the fabrication of the terminated transmission lines and in the Wilkinson splitter was evaporated NiCr (80/20% by wt). The NiCr was evaporated directly onto the InP and was delineated by conventional photoresist lift-off. Since the film resistivity is strongly dependent on the evaporation conditions, an in situ resistance monitor was used to determine the evaporation end point. The evaporated sheet resistivity was 80 to 90 Ω/square and the corresponding NiCr film thickness was between 300 and 500 Å. After the NiCr lift-off, Cr/Au (50 Å/8000 Å) transmission lines were evaporated and lifted. There was a 4-μm overlap of the NiCr resistor pattern and the Cr/Au transmission lines. After the NiCr and the Cr/Au patterns were in place, the NiCr was chemically etched to achieve a sheet resistance of 100 Ω/square.

The Lange coupler processing used a combination of lift-off and

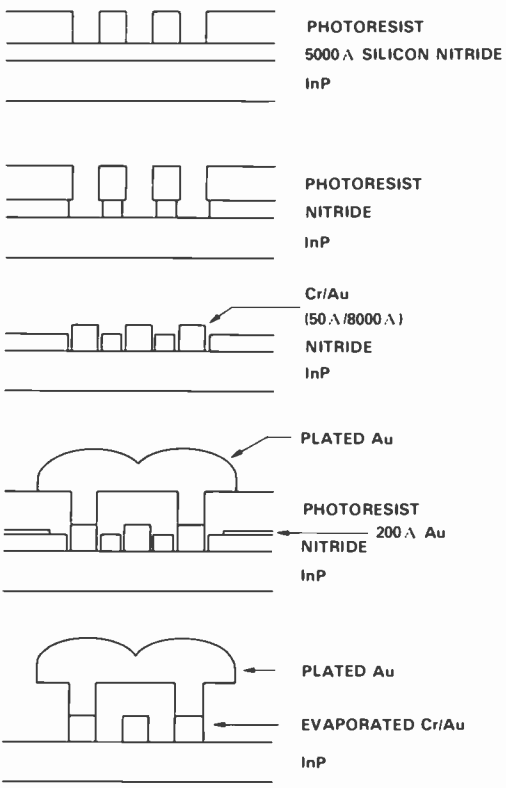

Fig. 2—Lange coupler air-bridge fabrication sequence.

plating technologies. The process sequence is outlined below and shown in Fig. 2. A 5000-Å silicon nitride film was deposited on the InP, and the first-level metallization pattern was printed in photoresist. The nitride was plasma etched, and then Cr/Au (50 Å/8000 Å) was evaporated and lifted. Undercutting of the nitride provided for a clean metallization lift-off, which was required to avoid shorting of the coupled lines. A thin Au film was then evaporated in the field to serve as a current path for Au electroplating. A 4 × 4 μm^2 air-bridge post pattern was printed in photoresist, and Au was plated in the post area. Plating was allowed to continue until the Au plating spread over the photoresist and joined. After plating, the photoresist was removed with acetone, and the thin gold in the field was removed by plasma etching. The structure at this step in the process, with the undercut nitride still in place, is shown in Fig. 3(a). The frontside processing was completed by removing the 5000-

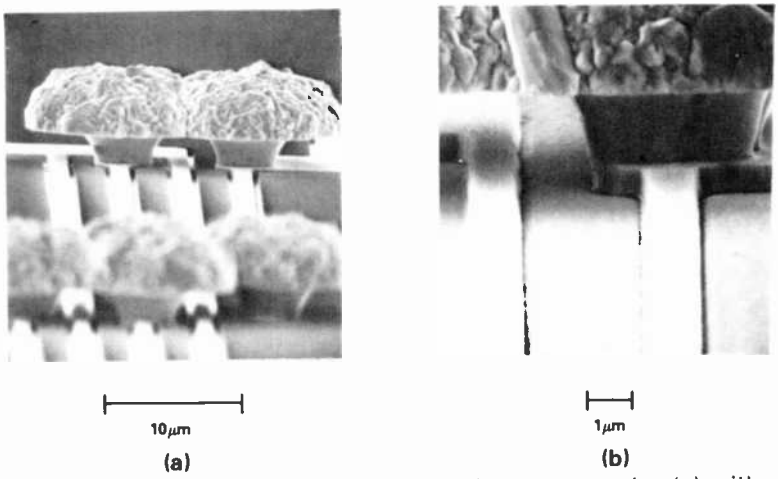

Fig. 3—Scanning electron micrographs of Lange coupler (a) with undercut nitride used for lift-off still in place and (b) with completed air bridge and nitride removed.

Å-thick nitride layer in buffered HF. The finished Lange coupler is shown in Fig. 3(b).

The final steps for both types of circuits are outlined below. After the completion of the frontside processing, the wafers were scribed and mounted on a sapphire disk by means of a low-temperature wax. The wafers were lapped to a thickness of 50 μm to establish the proper transmission-line impedances. After lapping, 1.5 μm of Al was evaporated on the backside of the wafers to serve as the microstrip ground plane. After the wafers were removed from the sapphire disk, the 1.6×1.6 mm^2 circuits were separated and mounted on brass blocks for millimeter-wave evaluation.

Test Results

The components were tested from 75 to 110 GHz. The circuits were interfaced to laboratory waveguide-measurement equipment through a microstrip-to-coaxial-to-waveguide transition.[12] The results presented here were de-embedded to remove the characteristics of the transitions and the microstrip losses.

The VSWR as a function of frequency of the terminated line is shown in Fig. 4. The VSWR is about 1.7 at the lower band edge, in reasonable agreement with the calculated lower-band-edge value of 1.4, and the shape of the curve agrees well with calculations that predict unity VSWR at the design band center of 112 GHz. The amplitude characteristics of the Wilkinson splitter are shown in Fig. 5. The power loss at each output arm with respect to the input

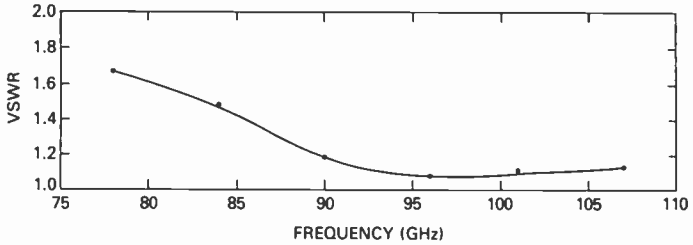

Fig. 4—Measured VSWR of the 50-Ω terminated line.

arm varies from 4 to 5 dB. As expected because of physical symmetry, the power split to each output arm was equal to within 0.5 dB. The VSWR of all three ports was less than 1.5, and the isolation between the two output arms was greater than 12 dB.

The amplitude and phase information for the Lange coupler is shown in Fig. 6. The top curve is the phase difference between the direct and coupled arms. The measured phase difference is close to the expected 90°. The middle curve is the power at the isolated arm with respect to the input arm. The isolation is greater than 13 dB across the 75- to 110-GHz band. The lower curves are the loss from the input port to the direct and coupled arms. The measured values, indicating a dissipation loss of 1 to 2 dB above the nominal 3-dB split, show reasonable agreement with the calculated values. The VSWR of all ports was better than 1.7.

Phase data for the sum/difference network are shown in Fig. 7. The ports of the sum/difference network are labeled in Fig. 1(d). For the input at port 2 and the output at ports 1 and 4, the phase difference at the output ports should be 180°. For the input at port 3, the output at ports 1 and 4 should be in-phase. The measured data for the 180° mode and the 0° mode are shown in Fig. 7. The

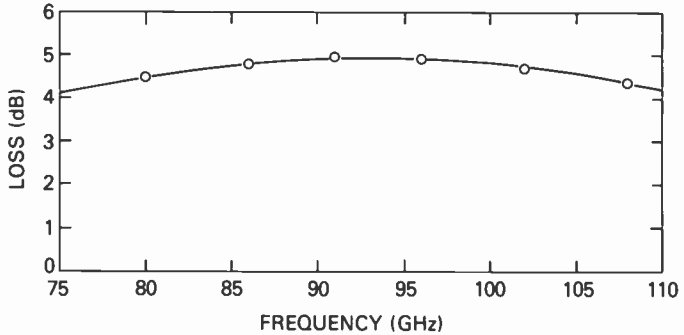

Fig. 5—Measured transmission loss to each output arm of the Wilkinson splitter.

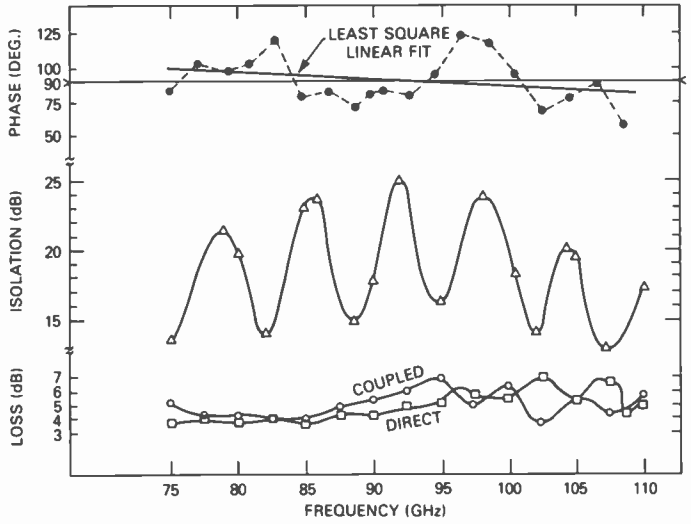

Fig. 6—Lange coupler 75- to 110-GHz evaluation. Top curve shows phase difference between direct and coupled arms; middle curve, loss from the input port to the isolated arm port; and bottom curves, loss from input port to coupled arm port and loss from input port to direct arm port.

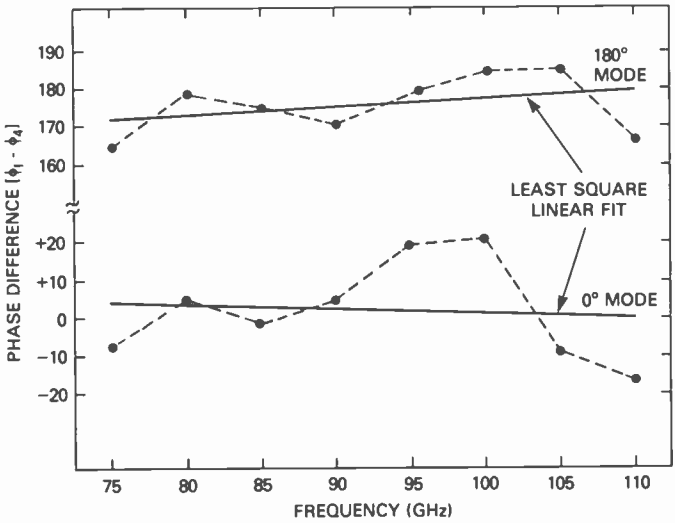

Fig. 7—Measured phase performance of the sum/difference network for 0° and 180° mode operation.

data in each case have been adjusted for a reference line length that is 21 μm longer than the design length, indicating a first iteration design error of only 6%.

Summary

Several microstrip passive circuit components have been designed, fabricated, and tested. The components consist of a terminated transmission line, a Wilkinson splitter, a Lange coupler, and a sum/difference network. The components were implemented in a microstrip format on 50-μm-thick InP substrates and cover the octave from 75 to 150 GHz. The fabrication of these components required the deposition of thin-film NiCr resistors, nitride-assisted lift-off techniques, and air-bridge formation. All of the components have provided good test results from 75 to 110 GHz. These components can now be directly incorporated with active devices to realize a wide range of millimeter-wave monolithic circuits.

Acknowledgment

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A Silicon Technology for Millimeter-Wave Monolithic Circuits*

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Abstract—A silicon millimeter-wave integrated-circuit (SIMMWIC) technology that includes high-energy ion implantation and pulsed-laser annealing, secondary ion mass spectrometry (SIMS) profile diagnostics, and novel wafer thinning has been developed. This technology has been applied to a SIMMWIC single-pole single-throw (SPST) switch and to IMPATT and p-i-n diode fabrication schemes. Thus, the SIMMWIC technology is a proven base for monolithic millimeter-wave sources and control circuit applications.

1. Introduction

The success of future millimeter-wave systems depends on the availability of reproducible, low-cost circuits. To date, millimeter-wave circuits have been commercially available as discrete components mounted in a waveguide, an inherently expensive transmission line medium. The silicon millimeter-wave integrated-circuit (SIMMWIC) technology offers a low-cost high-yield approach.[1-3]

Ingredients of the SIMMWIC technology are selective ion implantation, pulsed-laser annealing, secondary ion mass spectrometry (SIMS) profile diagnostics, and novel wafer thinning. The use of selective ion implantation and laser annealing over a part of the wafer assures that the high resistivity of the other parts is retained. This is essential for integrating millimeter-wave devices with low-loss microstrip circuits on silicon. Secondary ion mass spectrometry (SIMS) profile diagnostics provide the necessary feedback to coor-

* This paper is based in part on papers published in the *13th European Microwave Conference Proceedings*, 1983; *IEEE MTT-S Digest*, 1984; and *Electronics Letters*, 1984. See Refs. 1-3.

dinate the many ion implantations that make up the active device structures. Thinning a portion of the wafer to 2 or 3 μm is necessary to fabricate the all-ion-implanted IMPATT diode, as well as to minimize the thermal resistance.

In this paper, we demonstrate the first SIMMWICs. These monolithic circuits are single-pole single-throw (SPST) switches that operate in Q band (33–50 GHz). Performance includes 20% instantaneous 3-dB bandwidth, with a minimum isolation of 21.6 dB.

In addition, we describe a 60-GHz oscillator circuit utilizing 2000 $\Omega \cdot$ cm silicon wafers as substrates. This microstrip circuit, in conjunction with a discrete silicon IMPATT device, validates our monolithic in-silicon concept.

We also characterize, using cross-sectional transmission electron microscopy (TEM), the defects found in the regions of the silicon that were implanted with phosphorus at high energy and high dose. These implanted structures (implant energy of 1.5 MeV, fluence of 3×10^{15} atoms $\cdot$ cm^{-3}) are necessary for the creation of deep contact layers in the all-implanted IMPATT diodes.

In addition, we also demonstrate the fabrication of several types of p-i-n and IMPATT diodes by means of SIMMWIC technology. These include both vertical and horizontal (lateral) p-i-n diodes, as well as all-ion-implanted and laser-annealed IMPATT diodes.

2. High-Resistivity Silicon for Monolithic Sources

The use of high-resistivity silicon for monolithic circuits was first seriously investigated in 1965.[4] This approach was abandoned when it was found that the processing steps of epitaxial growth significantly lowered the resistivity of the silicon. To preserve the required high resistivity of the bulk silicon material, the processing temperature must not exceed 800°C. The techniques we are describing for processing and analyzing silicon wafers include ion implantation, laser annealing, SIMS, and TEM.[5,6] They permit fabricating the active devices without degrading the high-resistivity substrate. The high-resistivity silicon is then used as a substrate on which passive microstrip circuits are printed to complete the monolithic component for EHF.

3. SIMMWIC SPST Switch

An example of a monolithic circuit employing the SIMMWIC technology is a single-pole single-throw (SPST) switch, designed to operate in Q band (33–50 GHz). This switch incorporates an ion-im-

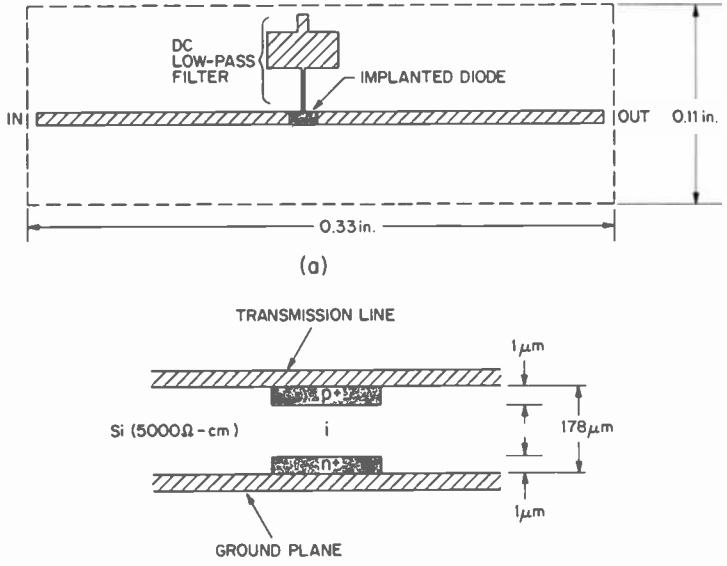

Fig. 1—SIMMWIC SPST switch. (a) Top view. (b) Side view.

planted, pulsed-laser-annealed p-i-n diode in shunt with a transmission line and a printed low-pass dc bias filter, all on the same high-resistivity silicon chip (Figs. 1 and 2). It can readily be incorporated into monolithic control circuits, such as phase shifters, limiters, and complex switching networks.

For millimeter-wave testing purposes, this silicon chip is placed in a groove whose cutoff frequency exceed 50 GHz to assure TEM-mode propagation. The ends of the chip protrude into the waveguide

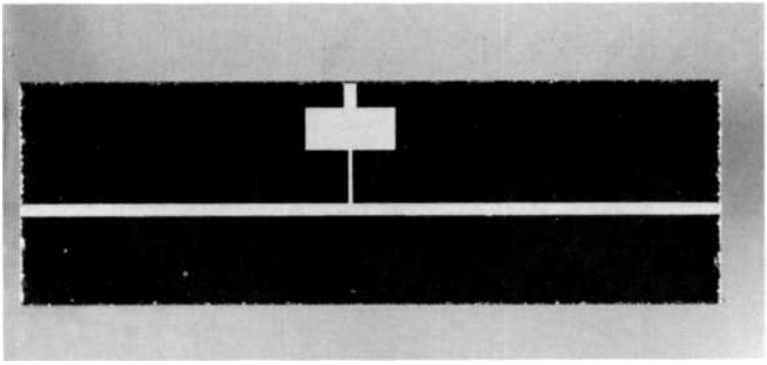

Fig. 2—Photograph of the SIMMWIC SPST switch.

Table 1—Switch Performance

f (GHz)	IL (dB)	ISOL (dB)	IL* (dB)	ISOL* (dB)
33.00	3.3	24.5	2.6	23.8
33.50	3.3	24.5	2.5	23.7
34.00	2.8	24.4	2.1	23.7
34.50	3.2	24.7	2.9	24.4
35.00	2.7	24.9	2.2	24.4
35.50	2.4	24.4	1.9	23.9
36.00	2.7	24.2	2.2	23.7
36.50	2.4	24.1	2.4	24.1
37.00	2.4	23.1	2.3	23.0
37.50	2.7	23.5	2.7	23.5
38.00	2.5	23.3	2.3	23.1
38.50	2.4	22.3	2.1	22.0
39.00	3.0	23.0	2.3	22.3
39.50	3.3	23.4	2.7	22.8
40.00	3.4	22.7	2.3	21.6
40.50	3.9	23.2	2.9	22.2

IL = Insertion loss (bias voltage is zero volts).
ISOL = Isolation (bias current is 100 mA).
IL* = Insertion loss corrected for transition and fixture losses.
ISOL* = Isolation corrected for transition and fixture losses.

to form E-probe transitions (the ground plane at the ends of the chip is etched off). First, sliding shorts tune the transitions for optimum bandwidth, then the shorts are fixed, and the measurements are made. Table 1 summarizes the measurements. After subtracting fixture and transition losses of up to 1 dB, the 3-dB bandwidth extends from 33 to 40.5 GHz (bias voltage is zero volts), and the minimum isolation is 21.6 dB (bias current is 100 mA).

The key advantages of this SIMMWIC SPST switch are small size, low cost, high yield, and large bandwidth. The actual monolithic circuit area including the dc filter is about 100 mils by 50 mils, and

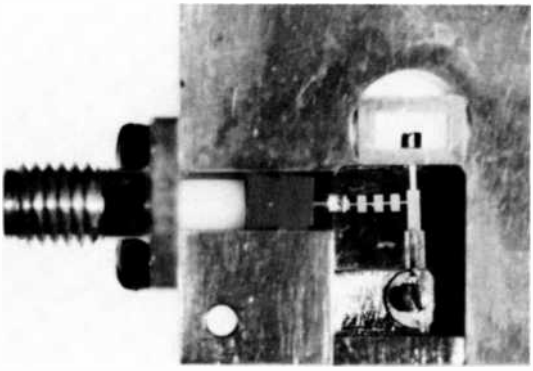

Fig. 3—Millimeter-wave hybrid-monolithic circuit on silicon.

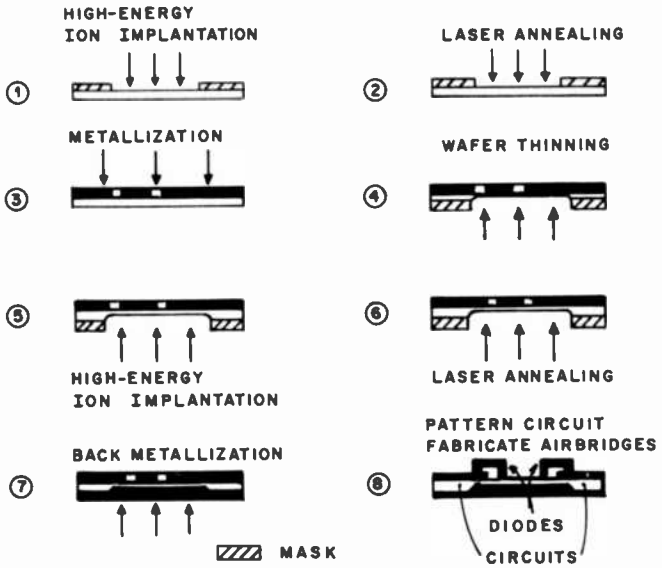

Fig. 4—Fabrication steps for silicon monolithic integrated circuits.

the substrate material is readily available silicon. The processing steps are reliable high-yield techniques, and the yield (based on static parameters) for the first run was about 90%. The shunt-mounted p-i-n diode switch realized in this manner is capable of operating over the waveguide band without any performance degradation.

4. Hybrid Monolithic Circuit Chip

To demonstrate the monolithic-circuit-in-silicon concept, we built a 60-GHz oscillator, using 2000-$\Omega \cdot$ cm silicon wafers as our substrate. This circuit, in addition to a discrete silicon IMPATT device in chip form, constitutes what we call the hybrid-monolithic source (Fig. 3). To measure the output power of the oscillator, an E-probe microstrip-to-waveguide transition circuit was employed. An output power of 12 mW at 60 GHz was attained.

Fig. 4 illustrates the fabrication steps for silicon monolithic circuits. In step 1, ions are implanted where the diodes are to be placed, and in step 2 the diodes are pulsed-laser annealed. In step 3, metallizaton is deposited on the back side, serving as a support, and in step 4 the device area is thinned chemically. The other side of the devices is implanted with high-energy phosphorus ion, and laser annealed in steps 5 and 6. After further metallization, the diodes

are completed, along with circuits at the edge of the wafer. Note that the substrate allocated for processing the circuits has been unharmed (since it never experienced high temperature); thus the devices can be made integral parts of the circuits.

5. TEM Annealing Study of Silicon Implanted with Phosphorus at High Energies

We have studied the worst possible conditions that can affect device properties, namely high-energy and high-dose ion implantation. It is important to note that the combination of high-dose and high-energy ion implantation is used only to create the contact layers of the IMPATT devices, the feasibility of which has been demonstrated. The drift region of the IMPATT diode may require high-energy implantation, but at a dose well below 10^{13} cm^{-2} (see Table 2 in Section 6.2). Therefore, no serious crystal damage is expected, and device properties will not be affected.

The damage found in the regions of the silicon implanted with high-energy phosphorus ions at a high dose before and after laser annealing have been characterized by transmission electron microscopy (TEM).

5.1 Ion-Implanted Sample Before Annealing

The first sample was ion implanted at 1.5 MeV with $^{31}P^{+}$ at a fluence of 3×10^{15} cm^{-2}. The SIMS profile of this sample is shown in Fig. 5. The as-implanted sample is shown in Fig. 6, where the cross-sectional specimen is viewed edge-on, with the free surface of the silicon facing the top of the page. Centered 1400 nm below the surface, three alternating bands of contrast can be observed. The central bright band represents an amorphous region in the silicon, while the bounding dark bands result from regions of distorted crystallinity.

The photograph in Fig. 6 was taken in a symmetric [011] condition (i.e., the optical axis of the microscope and the crystallographic [011] pole coincided). In this orientation, several planes are in approximate Bragg diffracting conditions, producing a moderately strong diffraction of the main beam out of the objective aperture (electrons diffracted out of this aperture are not imaged). The dark bands bounding the amorphous layer are presumably due to the disorder in these regions, which relaxes the Bragg conditions and results in a stronger diffraction of the main beam. Within the amorphous region, diffraction does not occur due to the lack of crystalline

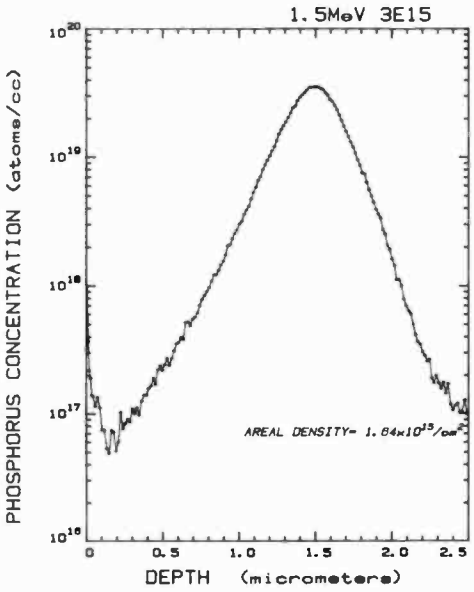

Fig. 5—SIMS of the 1.5-MeV ion implantation.

structure. The main beam is less strongly attenuated, causing the bright contrast in this region. The amorphous band extends from 1270 to 1530 nm below the surface of the wafer. The disordered layers extend 130 nm below and 200 nm above the amorphous region.

Fig. 7 is a dark-field image formed by imaging a diffracted beam. In this image, the amorphous layer is dark since electrons passing

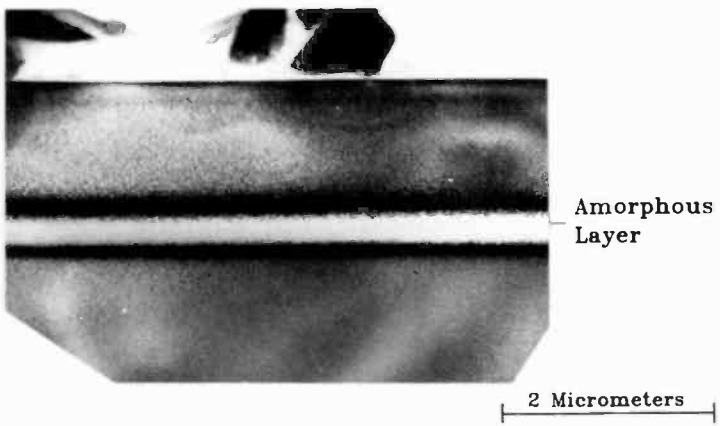

Fig. 6—Cross-sectional TEM before annealing.

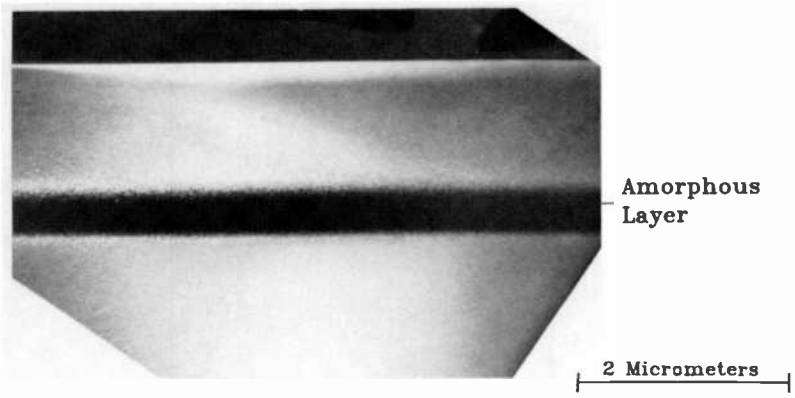

Fig. 7—Dark-field cross-sectional TEM before annealing.

through this region are not diffracted. The crystalline regions below and above the amorphous layer display contrasts similar to each other, indicating that they are in the same crystalline orientation.

5.2 Laser-Annealed Sample

The second sample was implanted with $^{31}P^{+}$ at 1.5 MeV and a fluence of 3×10^{15} cm^{-2}, and at 1.0 MeV and a fluence of 1×10^{15}

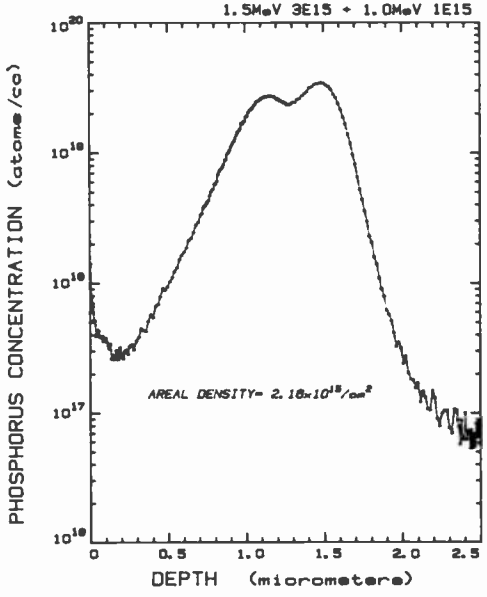

Fig. 8—SIMS of the 1.0-MeV and 1.5-MeV ion implantations.

cm^{-2}; it was also laser annealed with an energy density of 1 joule · cm^{-2} at 1.06- and 0.53-μm wavelengths for a duration of four 15-nm pulses. The SIMS profile is shown in Fig. 8, and the defect structure of the laser-annealed sample is shown in Fig. 9.

Three distinct levels can be observed within the implanted region. The upper level extends from the sample surface to a depth of 200 nm and appears to be a region of the crystal that has undergone melting and liquid-phase recrystallization. The V-shaped structures have previously been reported for laser-annealed liquid-phase epitaxy by Cullis.[7] The middle level extends from 200 to 870 nm and consists of the remains of the single-crystal region through which the implanted ions have passed. The lowest level extends from 870 to 1500 nm and is composed of polycrystalline silicon grains formed from the amorphous layer upon laser annealing. This evidence of crystallization substantiates the use of high-energy, high-dose laser-annealed layers.

6. IMPATT Diode

6.1 Double-Drift Structure with Only the Contact Implanted

The first step in determining the validity of the ion-implantation and laser-annealing techniques for millimeter-wave devices is the use of these techniques in the processing of the contact layer.

First, n and p layers are grown epitaxially on top of an n^+ arsenic-doped substrate, creating the two drift regions. To complete the

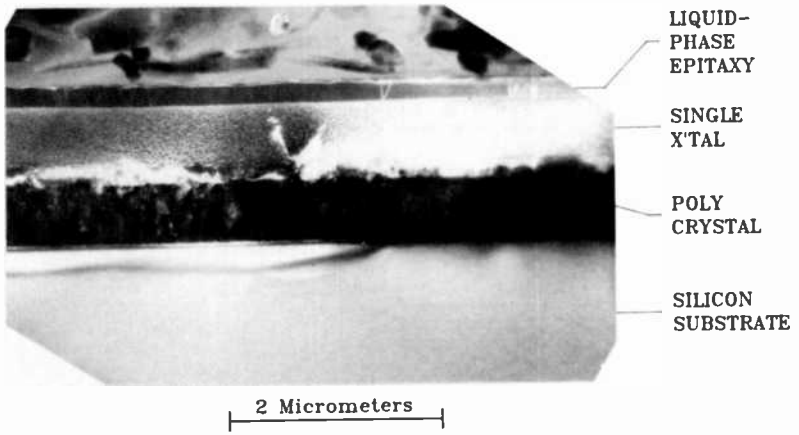

Fig. 9—Cross-sectional TEM after pulsed-laser annealing.

device structure, ^{11}B is implanted with an energy of 40 keV and a dose of 1.0×10^{15} cm^{-2} and then laser annealed. Devices with a power output of over 450 mW at 44 GHz were fabricated and have demonstrated a yield (based on static parameters) of over 90%. The use of ion implantation and pulsed-laser annealing to create contact layers has become the preferred technology in our laboratory, and devices operating up to 200 GHz have been reported.[8]

6.2 Double-Drift Structures with One Contact and One Drift-Region Implanted

In the next step, we demonstrate preliminary rf results from double-drift IMPATT diodes in which one contact and one of the two drift regions were fabricated by ion implantation and pulsed-laser annealing (Fig. 10).

These diodes were fabricated by epitaxially growing an n-type (arsenic) drift region on a substrate heavily doped with arsenic. The growth of the n-type drift region was followed by an epitaxially grown lightly arsenic-doped (1×10^{15} cm^{-3}) layer. At this point, SIMS analysis was performed (Fig. 11); it indicated a doping level

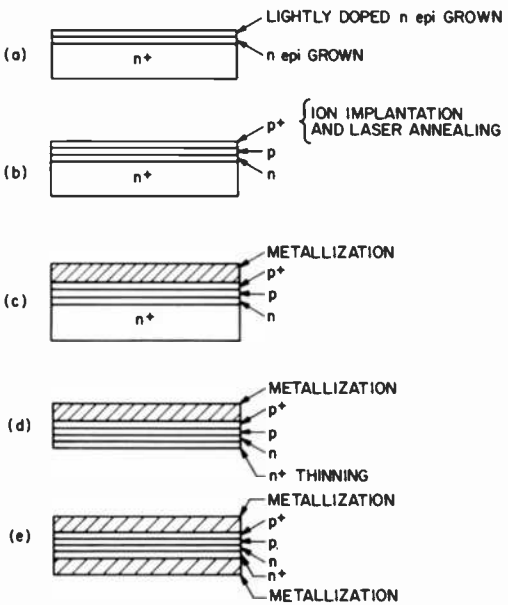

Fig. 10—Fabrication of double-drift IMPATT diodes by SIMMWIC technology.

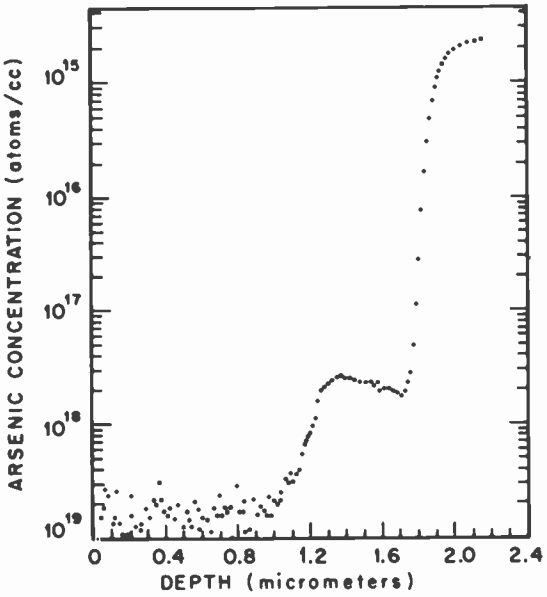

Fig. 11—SIMS of the partially completed double-drift structure with one drift region implanted.

in the drift region much lower than desired ($2.5 \times 10^{16}\,cm^{-3}$). Based on this data, a matching n-type drift region and a contact region were ion implanted into the lightly doped epitaxial layer (Table 2). The SIMS profile before and after laser annealing is shown in Fig. 12. Laser annealing does not alter the impurity concentration profile; however, boron channeling prevents a flat p-type drift region from being formed.

Subsequently, the wafers were metallized and thinned, and the diodes were defined. The diodes have a breakdown voltage of 42 V (defined at 1 mA). RF measurements show output power in excess of 96 mW at 43 GHz in a WR-22 radial-cap-type waveguide cavity.

These results clearly demonstrate the viability of a pulsed-laser-

Table 2—Double Drift Structure with One Drift Region Implanted

Implant No.	Side	Ion	Equivalent Energy (keV)	Equivalent Dose (Atoms · cm^{-2})
1	I	B	50	1.54×10^{15}
2	I	B	240	3.16×10^{11}
3	I	B	350	4.86×10^{11}
4	I	B	480	6.67×10^{11}

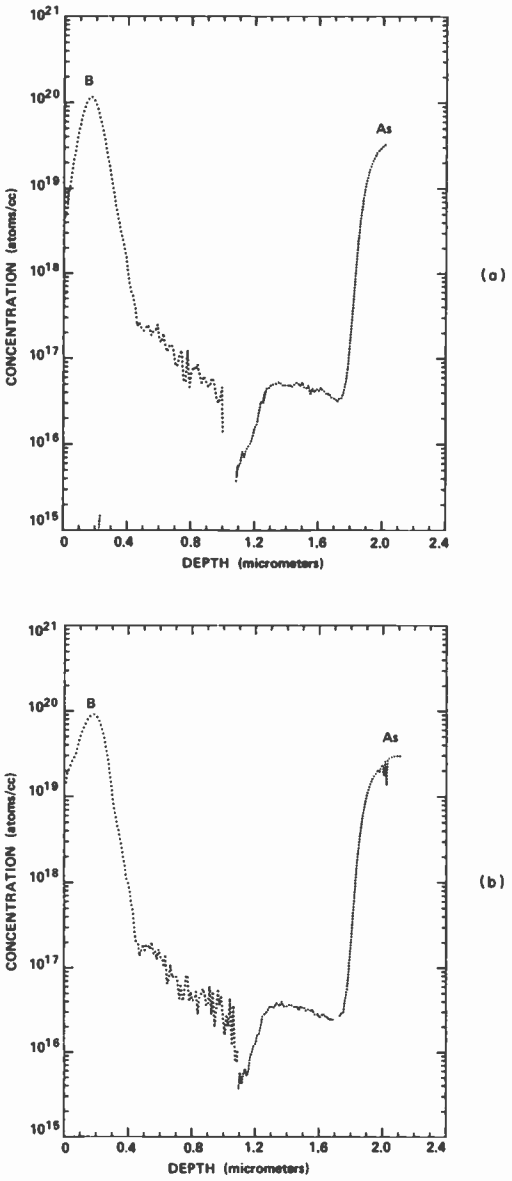

Fig. 12(a)—SIMS of the double-drift structure with one contact and one drift region implanted only.

Fig. 12(b)—SIMS of the double-drift structure with one contact and one drift region implanted and also laser annealed.

annealed ion-implanted drift region, designed and tailored with the aid of SIMS.

6.3 Single-Drift All-Implanted Structure

We have carried out preliminary studies to demonstrate the feasibility of fabricating p-n junctions from high-energy (MeV) ion implantation into a high-resistivity substrate. This was followed by laser annealing to activate the area while preserving the high-resistivity property of the substrate.

Fig. 13 is the carrier concentration profile of a p-n junction achieved by boron and high-energy phosphorus implants into a high-resistivity silicon substrate. After the ion implantations, the silicon wafer is pulsed-laser annealed to activate the p and n layers. Because the pulse is relatively short (15 ns), the laser heats and anneals only about 3 μm from the silicon substrate surface, without causing any degradation in the high resistivity of the bulk substrate. Fig. 14 shows the *I-V* characteristics of the p-n junction diode formed by this process. Both the reverse-breakdown and forward-conduction characteristics are comparable with those of epitaxial p-n diodes.

Fig. 15 depicts the SIMS profile of an alternative approach, an all-implanted, complementary, single-drift IMPATT. Here the p-

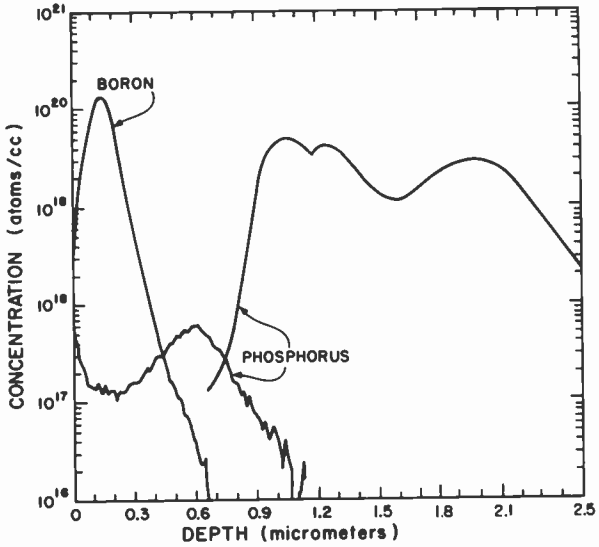

Fig. 13—Composite SIMS of the all-implanted single-drift structure.

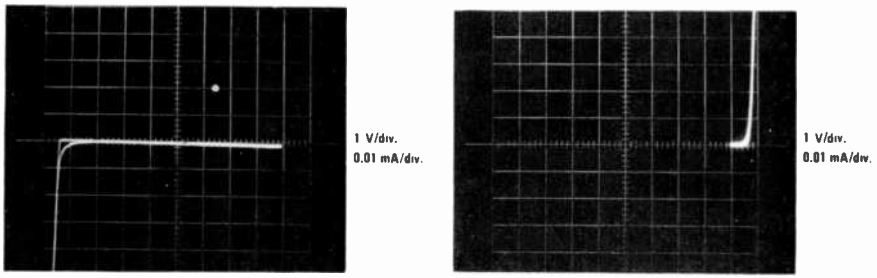

Fig. 14—*I-V* characteristic of the p-n junction.

type drift region was created by implanting ^{11}B. Table 3 gives an implantation summary of this all-implanted IMPATT.

6.4 Double-Drift All-Implanted Structure

We also fabricated all-ion-implanted and laser-annealed double-drift IMPATT diodes from a 5000-Ω · cm silicon substrate. The various fabrication steps are shown in Fig. 16.

The SIMS of this structure (side I only) is shown in Fig. 17; the ion-implantation steps are summarized in Table 4; and the resulting *I-V* characteristic of this diode is shown in Fig. 18.

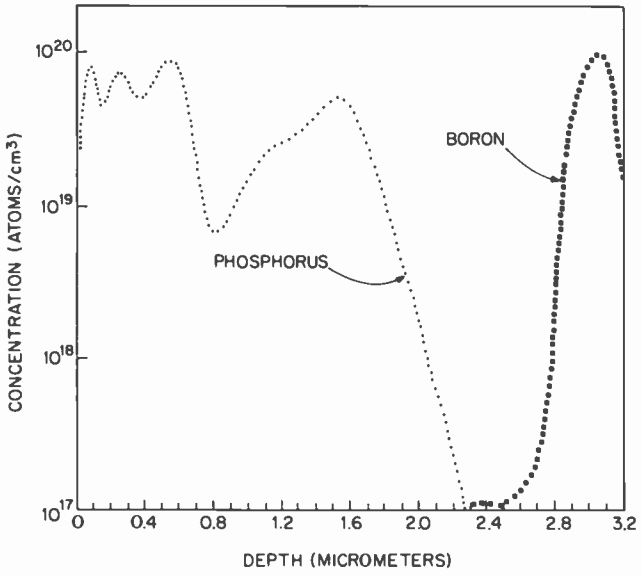

Fig. 15—Composite SIMS of the all-implanted complementary single-drift structure.

Table 3—Single-Drift All-Implanted Complementary Structure

Implant No.	Side	Ion	Equivalent Energy (keV)	Equivalent Dose (atoms · cm^{-2})
1	I	B	50	1.54×10^{15}
2	I	B	200	1.20×10^{12}
3	I	B	300	1.21×10^{12}
4	I	B	400	1.43×10^{12}
5	II	P	1500	3.0×10^{15}
6	II	P	1000	1.0×10^{15}
7	II	P	400	2.55×10^{15}
8	II	P	180	1.26×10^{15}
9	II	P	60	6.37×10^{14}

The experiments described in Sections 6.1 to 6.4 clearly demonstrate the feasibility of achieving both p and n layers from high-resistivity silicon substrates while preserving the bulk high-resistivity property of the substrate.

7. p-i-n Diode

Mesa p-i-n diodes were fabricated by means of ion implantation and laser annealing. The various fabrication steps are shown in Fig. 19. The breakdown voltage exceeds 400 V, and the C-V measurements

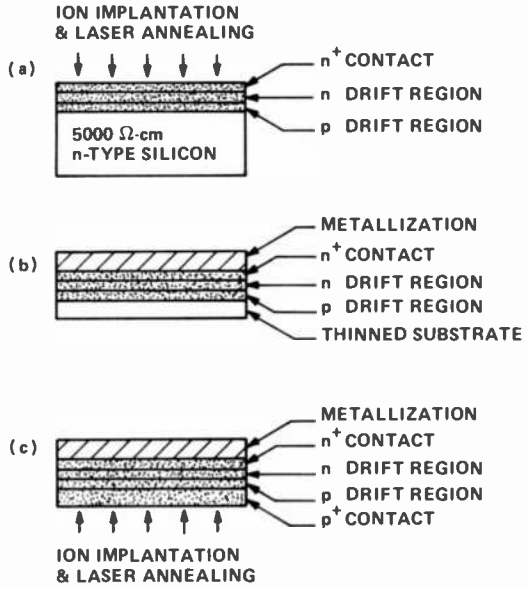

Fig. 16—Fabrication of the all-implanted double-drift structure.

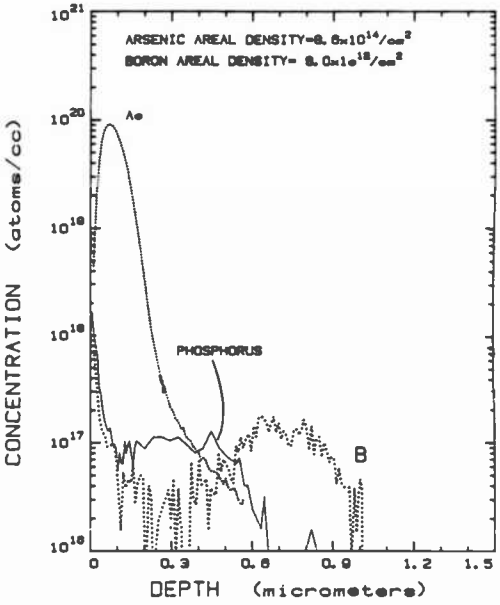

Fig. 17—SIMS of the double-drift, all-implanted structure.

indicate that full depletion of the i layer occurs at a bias voltage (V_B) of -1 V. The C-V characteristics of a typical diode are shown in Table 5 and plotted in Fig. 20.

In fabricating lateral p-i-n diodes, aligned masks were used to first implant the p^+ contact and then the n^+ contact into 5000-$\Omega \cdot$ cm n-type silicon. The wafers were then annealed, and the metal contacts were defined. The first run was annealed by conventional high-temperature techniques, with a diode breakdown voltage (at

Table 4—Double-Drift All-Implanted Structure

Region	Side	Ion	Equivalent Energy (keV)	Equivalent Dose (atoms · cm^{-2})
1	I	As	90	3.31×10^{14}
2	I	As	150	4.93×10^{14}
3	I	P	170	9.67×10^{11}
4	I	P	270	1.49×10^{12}
5	I	P	400	2.55×10^{12}
6	I	B	220	2.96×10^{12}
7	I	B	320	2.45×10^{12}
8	II	B	400	1.00×10^{15}
9	II	B	190	2.83×10^{15}
10	II	B	60	1.71×10^{15}

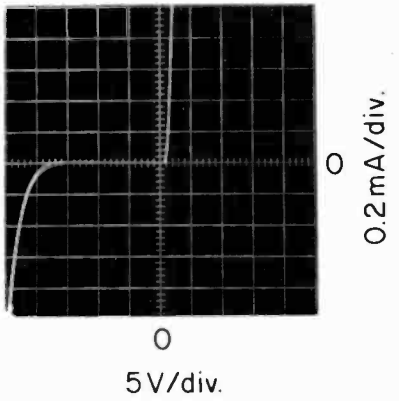

Fig. 18—*I-V* characteristic of the double-drift, all-implanted structure.

I_R = 10 μA) of 700 V. The second run was laser annealed with similar results. Fig. 21 depicts a typical lateral p-i-n diode in a series configuration with a transmission line, ideally a silicon microstrip line.

8. Conclusion

The first SIMMWIC has been successfully fabricated. This circuit is a monolithic SPST switch with a 3-dB bandwidth of 20% and a minimum isolation of 21.6 dB across the band (center frequency is 36.75 GHz). This monolithic circuit is a low-cost, reproducible foundation for all millimeter-wave control applications.

SIMMWIC technology was used to fabricate microstrip-line oscillator circuits on silicon, and various types of IMPATT and p-i-n

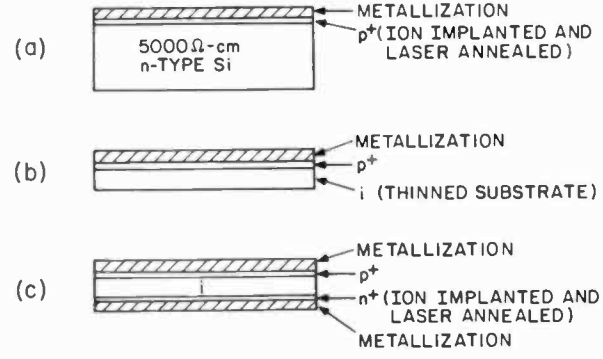

Fig. 19—Fabrication of p-i-n diodes by SIMMWIC technology.

Table 5—Mesa p-i-n C-V at 1 MHz

V (V)	C (pF)	V (V)	C (pF)
0.35	0.889	−0.59	0.075
0.30	0.669	−1.05	0.069
0.20	0.257	−4.0	0.068
0.10	0.138	−14.0	0.062
−0.26	0.095	−149.0	0.060

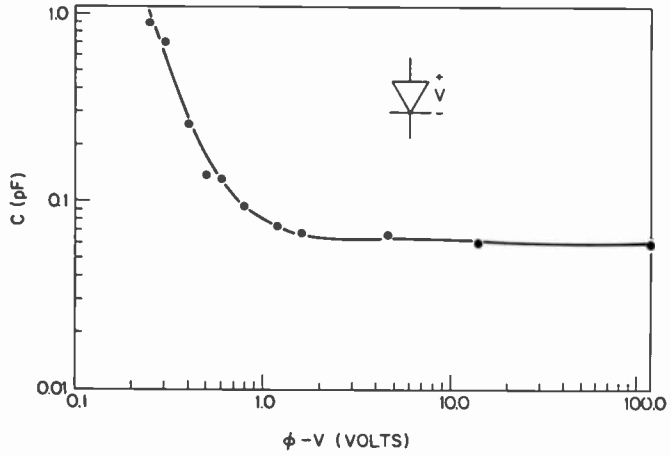

Fig. 20—C-V characteristic of a p-i-n diode made by SIMMWIC technology (V is the applied bias voltage; ø, the built-in junction potential, is 0.6 V).

diodes. An output power of 12 mW at 60 GHz was attained from a hybrid monolithic source; 96 mW at 43 GHz was achieved from a double-drift IMPATT diode with one drift region and one contact region fabricated by ion implantation and pulsed-laser annealing.

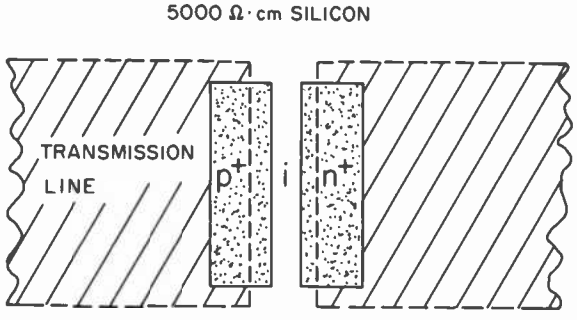

Fig. 21—Lateral p-i-n diode in a series configuration.

Single- and double-drift all-implanted diodes have been made from high-resistivity substrates by ion implantation, laser annealing, and novel wafer thinning. Lateral- and mesa-type p-i-n diodes have also been made by means of this technology. *We have demonstrated that SIMMWIC technology is useful for complete millimeter-wave subsystem integration.*

Acknowledgments

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A GaAs Power FET Suitable for Monolithic Integration, with Laser-Processed Gate and Drain Via Connections

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Abstract—A new microwave device format that combines flip-chip and via-connection technologies is described. This approach avoids many of the compromises inherent in conventional microwave monolithic circuits and will be particularly important in power applications. This paper reviews the rationale for this device format and describes a novel method of forming via connections through thick ($H < 0.37$ mm) semi-insulating substrates by a laser-drilling technology.

Preliminary discrete flip-chip devices with gate and drain via connections have been fabricated, and results have been obtained through 18 GHz. At 12 GHz, an output power of 308 mW at 28% power-added efficiency and 4.5-dB power gain have been achieved with a single-cell (0.6 mm/cell) GaAs FET. At 15 GHz, two 0.6-mm-width cells were lumped-element matched and combined, and an output power of 448 mW was obtained with 19.7% power-added efficiency and 4-dB gain. Efficiencies as high as 31% were achieved with these preliminary devices.

Introduction

In a conventional monolithic microwave circuit,[1] such as that illustrated in Fig. 1(a), a via connection[2] is made between the device source contact and a metal heatsink. This necessitates unavoidable performance compromises because of contradictory substrate-thickness requirements. In power applications, a low thermal resistance is necessary to maintain low operating-channel temperature for im-

proved device reliability. Since semi-insulating GaAs is a poor heat conductor, satisfactory thermal properties can be achieved only by minimizing the GaAs thickness between the device channel and heatsink. A thin substrate is also desirable for a low source inductance, since any inductance between the device source contact and ground degrades the transistor maximum available gain. This effect is particularly important for large-width power devices, where the gain reduction is more evident, and at high frequencies, where gain is limited.

For example, in commercially available discrete power FETs, when a source via format is used, the substrate is generally thinned to a thickness of 25 to 50 μm to realize the lowest possible thermal resistance and source inductance. However, circuit elements that are also printed on the semi-insulating GaAs substrate, and which propagate waves in a quasi-TEM mode, require thick substrates for low transmission loss. In general, the thicker the substrate the lower the insertion loss, provided other modes of propagation are not excited. Gopinath[3] has shown, for a given frequency and relative dielectric constant, that when radiation modes are taken into account there exists an optimum substrate thickness for maximum Q of a microstrip resonator. Fig 2 shows a plot, based on Gopinath's analysis, of the optimum substrate thickness for maximum Q for GaAs ($k = 13$). At 50 GHz, the optimum substrate thickness is 0.1 mm, which is the nominal thickness chosen in conventional monolithic circuits. For frequencies below 50 GHz, thicker substrates are desirable and conventional MMICs are nonoptimum from a circuit point of view.

An alternate device format that circumvents this problem is shown in Fig. 1(b). The device is flip-chip mounted,[4] and via con-

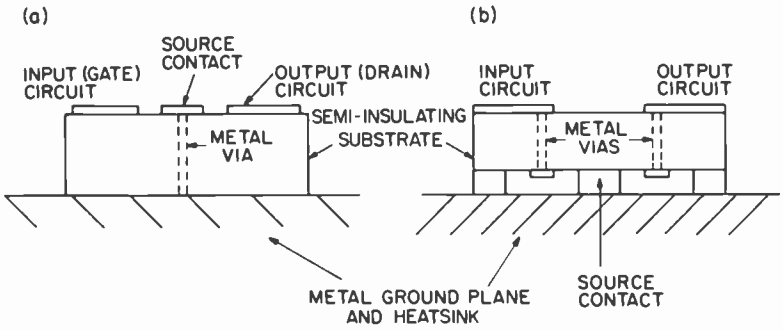

Fig. 1—Monolithic circuit approaches: (a) conventional format with a source-via connection and (b) flip-chip format with gate- and drain-via connection.

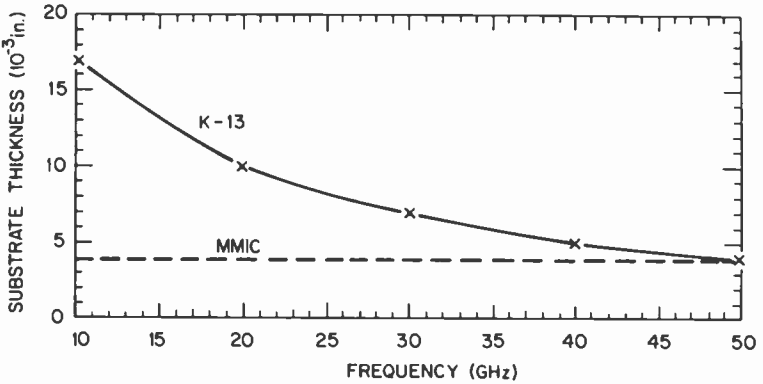

Fig. 2—Optimum thickness versus frequency for 50-Ω half-wave microstrip resonator on a GaAs (k = 13) substrate.

nections are made through the substrate to the gate and drain pads.[5] A thick source contact is used to provide the height differential required to prevent the gate and drain contacts from shorting to ground when the device is bonded to its heatsink. The source inductance and thermal resistance are then *independent* of the substrate thickness, and depend only on the device gate-to-gate spacing and the source-contact dimensions. Thick substrates can therefore be used to realize high-Q circuits on the back of the substrate. Since the source contact elevates the substrate from ground, circuit elements can also be printed on the *same* side as the device. The properties of the device and passive circuit can thus be optimized independently without any compromises, provided that via connections can be formed through thick ($H < 0.375$ mm) substrates.

Via Processes

There are several methods of producing via holes through GaAs substrates. Although wet chemical etching is currently the most widely used process, plasma etching and laser drilling offer several advantages. The main characteristics of each of these processes are compared in Table 1. Wet chemical etching is popular because it is a batch process employing simple equipment. Chemical etching usually produces holes with sloping sidewalls that allow an evaporated metal layer to adequately "seed" the gold plating used to establish the electrical connection. For a given wafer thickness, the lateral undercut of wet etching limits the spacing that can be used between via holes. Chemical etching also offers little tolerance to overetching, thereby placing stringent requirements on wafer-thickness

Table 1—Advantages and Disadvantages of Different Via Processes

Wet Chemical	Plasma or RIE	Laser
	Advantages	
Batch process	Batch process	Vertical sidewalls
Simple equipment	Vertical sidewalls	Very thick substrates possible
Sloped sidewalls allow easy plating	Overetching possible	Closely spaced vias possible
	Closely spaced vias possible	Conductive sidewalls aid plating
	Disadvantages	
Undercut limits wafer thickness and via spacing	Plating difficult (photoelectrochemical plating necessary)	Deposition of debris
Overetching difficult	Masking-layer erosion limits wafer thickness	Localized heating
Uniform etch rate difficult		Sequential process (can be automated)

uniformity. For very thick substrates, it is difficult to supply fresh etchant to the inside of the via holes, so the etch rate tends to decrease with time, and nonuniform etch rates may result.

Plasma etching and reactive-ion etching (RIE) are batch processes that, under proper conditions, eliminate most of the lateral undercut, achieving nearly vertical sidewalls. This allows improvement in the allowable via-to-via spacing and permits overetching to be used to compensate for thickness variations across the wafer. There are, however, several restrictions. These processes are usually restricted to thin substrates and, thus, limited by masking-layer erosion in the plasma. For deep holes, a metal layer evaporated on the near-vertical sidewall does not form a continuous layer, as is necessary for gold plating. Also, if the via hole terminates on a metal layer on the front of the wafer, it can be difficult to avoid trapping air when placing the wafer in the plating bath. Last, preferential plating close to the top edge of the via hole can lead to poor sidewall coverage and trapping of plating solution. To combat these problems, photoelectrochemical plating has been employed with some success.

Laser drilling of via holes is attractive when thick substrates or closely spaced via holes are desired. The depth of the via hole is determined by the energy of the laser employed and by the mechanism by which the vaporized material escapes from the hole. It is difficult to adjust the laser system to penetrate the GaAs substrate and avoid penetrating a thin metal layer on the front side of the

wafer, so the via holes form a tube open on both sides of the substrate. For GaAs, the laser-drilling process produces a conductive sidewall that is adequate to initiate gold plating directly on the untreated hole.

The main disadvantages of laser drilling are possible damage from localized heating, and the deposition of debris. Also, laser drilling is a sequential process. However, because the time to drill each hole is extremely short, automatic wafer positioning can improve the throughput.

Laser-Drilled Via Connections

We have discussed earlier[5] how a laser can be used to form via connections through thick semi-insulating GaAs substrates without the need for chemical etching.[6]

A 1.06-μm *Q*-switched Nd-YAG laser-trimming system (Quantronix 112B) is used. As shown in Fig. 3, the hole diameter is a nearly linear function of the power to the incandescent pump lamps over the range 2.4–3.0 kW. Fig. 3 shows the via-hole diameters obtained with 6.5× and 10× objective lenses. Since the 10× objective reduces the laser spot size more than the 6.5×, higher input

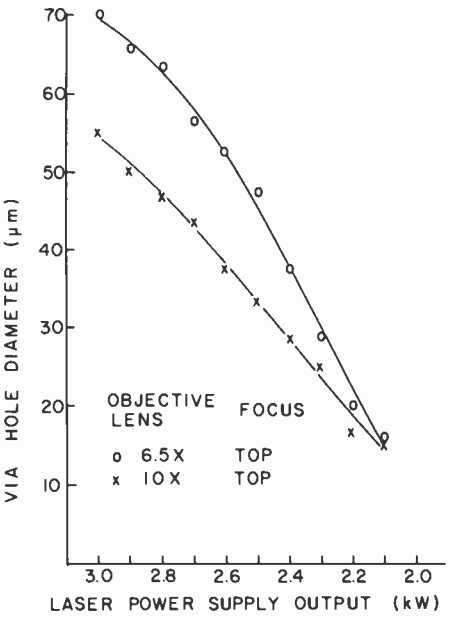

Fig. 3—Via-hole diameter versus laser flash-lamp power.

power is required to generate the same diameter hole. For the 6.5× objective, with substrates as thick as 0.38 mm, a lamp power of 2.5 kW (laser output of ~5 W) yielded 20-μm diameter holes. A hole diameter of 70 μm was obtained at the maximum lamp power of 3.0 kW (laser output of ~7 W). For a given pump-lamp power setting, the variation of hole diameter was typically ±5 μm. Fig. 4 shows a cleaved cross section of a 0.23-mm-thick substrate in which 23-μm diameter holes with vertical walls were drilled.

Unlike chemical etching, laser drilling shows surface damage and redeposited material at both the entrance and the exit holes, with more debris appearing around the entrance hole. The debris can be minimized by adjusting the laser system and by carefully cleaning the substrate after drilling. The extent to which the damage extends laterally from the via hole was assessed indirectly by monitoring the dc characteristics of the active device before and after drilling. No degradation was observed for laser-drilled holes spaced as close as 50 μm from the active device channel.

The principal processing steps used to fabricate via connections to the gate and drain pads are illustrated in Fig. 5. The process starts after the active devices have been fabricated on the front side of the wafer.[7] The wafer is then lapped and polished to the final substrate thickness desired. With an infrared aligner, a photoresist pattern is produced on the back of the wafer, and alignment keys are chemically etched to register the via-hole locations to the device pattern. A conductive, thin titanium-and-gold layer is deposited on the wafer back to assist in gold plating. Thick photoresist is applied to both sides of the wafer and patterned on the back-side surface with a via-hole mask and on the device side with a combination of

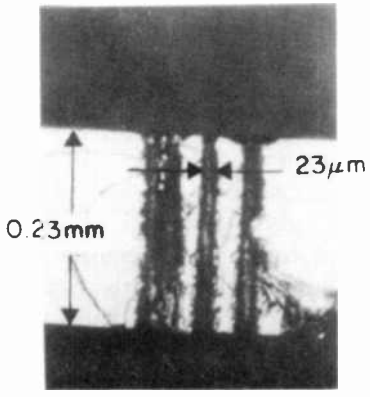

Fig. 4—Laser-drilled via holes.

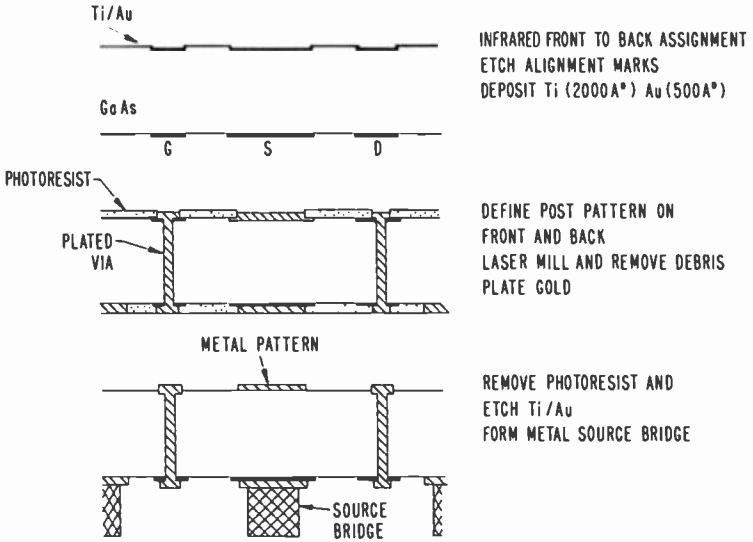

Fig. 5—Principal process steps used to fabricate via connections to the gate and drain pads.

source-post and gate- and drain-pad patterns. The pattern on the back of the wafer can also incorporate features to produce matching elements or cell interconnection lines. Holes are then laser drilled from the back of the wafer to avoid heavy debris deposition on the active device side. Chemical cleaning in a dilute solution of hydrogen peroxide removes some redeposited material without removing the conductive sidewalls obtained from laser drilling. Some debris is trapped by the photoresist layers and is removed after the gold plating. After the chemical cleaning, gold is electroplated to fill in the via holes and make the back-to-front connection. After plating, the Ti/Au layer on the back of the wafer is etched off to isolate the devices. The fabrication process is completed by patterning thick photoresist on the front of the wafer and plating a source-bridge interconnection.

The uniformity of the gold plating along the via hole is important in achieving low-resistance connections. We investigated the plating uniformity by angle-lapping substrates with a large number of via connections. The via-connection cross section as a function of depth through the wafer was thus determined. Fig. 6 shows a cross section obtained for nominal 50-μm-diameter vias near the center of a wafer and close to the entrance and exit sides. The plating is

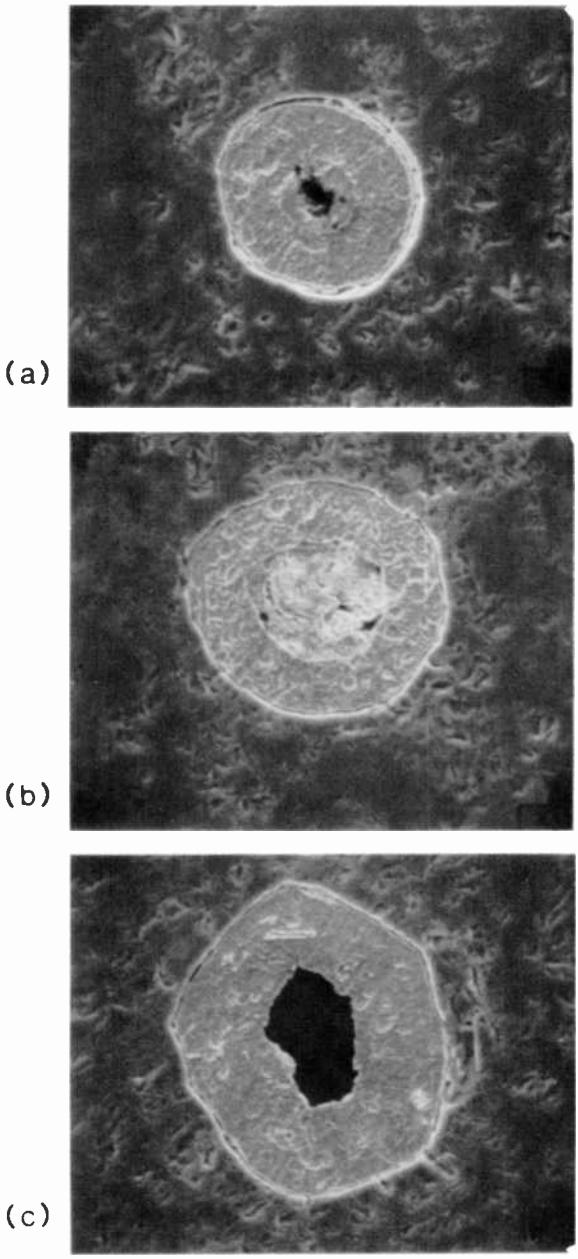

Fig. 6—SEM photographs at 1000× of gold-plated via holes cross-sectioned by angle lapping at 1°. Via-hole cross sections are (a) near exit side, (b) near wafer center, and (c) near the entrance side of the laser-drilled hole. Laser power = 2.6 kW.

about 14 μm thick at the wafer center, and increases to about 18 μm at the entrance and exit surfaces. To reduce this effect, the current density during plating is kept low to avoid localized depletion of the plating solution.

Fig. 7 is a photograph of a processed wafer in which a section was etched back to expose the via connections. The plated via connections, 23 μm in diameter and spaced 300 μm apart, are very uniform. The hole drilled by the laser acts as a form for the plated metal and determines the via diameter. The plated gate and drain pads are visible in the unetched wafer section. The pad dimensions in this photograph are 75 μm × 85 μm, which illustrates that very accurate placement of vias across a wafer is possible. Between gate and drain pads, a metal pattern that emulates the FET source-post pattern on the device side of the substrate is also visible. These patterns are currently being used as experimental tuning elements.

Discrete Via Devices

Fig. 8 is a photograph of the device side of a completed GaAs power FET chip with laser-drilled via holes connecting the gate and drain pads to the back side of the semi-insulating substrate. The chip is organized in a two-cell, 0.6-mm-per-cell pattern. Each FET cell is capable of generating a saturated output power of 0.25 W and contains four 75-μm unit-width gate fingers. The devices have an interdigitated, source-over-gate-and-drain geometry with a 47-μm

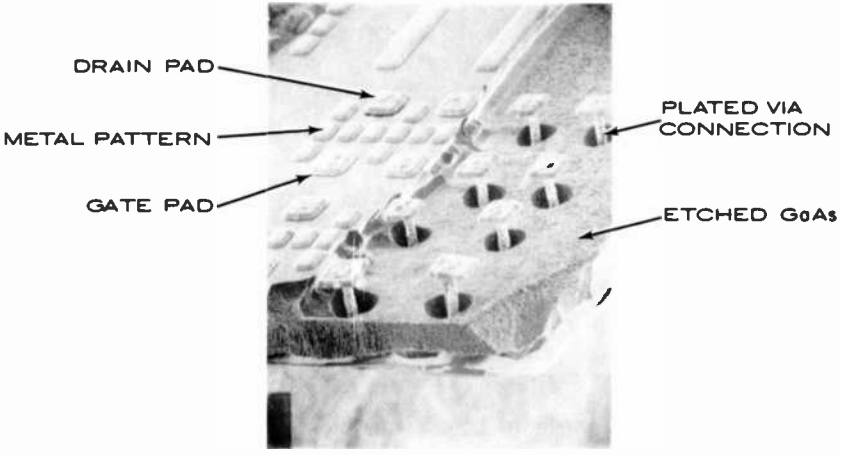

Fig. 7—Photograph of a processed wafer in which a section has been etched back to expose the via connections.

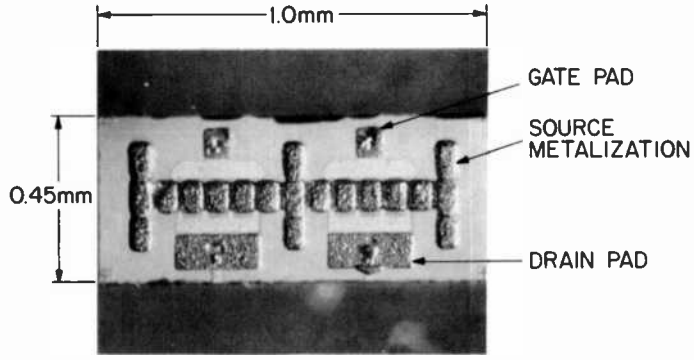

Fig. 8—Photograph of the device side of the power FET chip with gate and drain via connections.

source width, 25-μm drain width, and a source-to-drain channel width of 4.5 μm. The total chip dimensions are 0.45 mm × 1.0 mm.

Fig. 9 is a photograph of the chip with via holes flip-chip-mounted onto a copper heatsink. The thick source metalization elevates the gate pad by approximately 40 μm. The gate and drain pads on both sides of the 180-μm substrate are connected with 25-μm-diameter via connections. The device is mounted onto the heatsink (and electrical ground) using a fluxfree soldering technique. A small amount

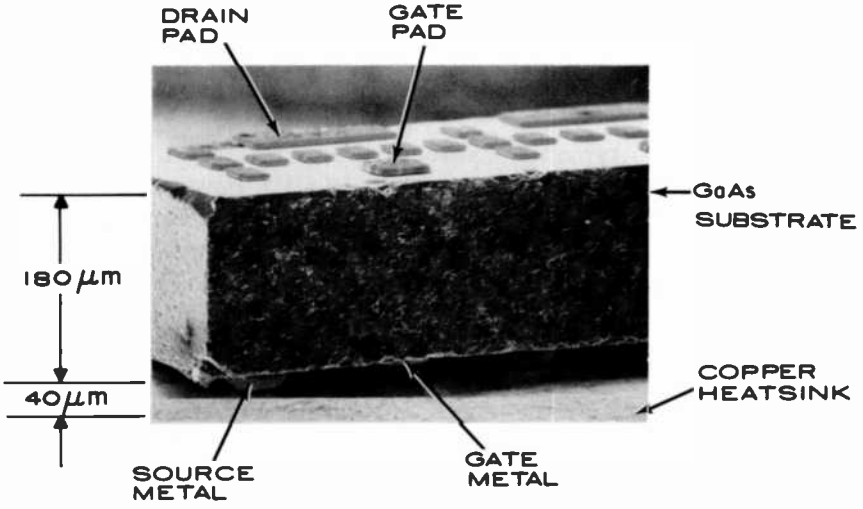

Fig. 9—Photograph of a flip-chip GaAs power FET with gate and drain via connections bonded to a copper heatsink.

of flux is used to flow a solder preform over the metal surface where the FET is to be placed. The flux is then cleaned off, and the device is mechanically placed onto the solder by means of a split-optics flip-chip machine. The chip is fired in a hydrogen atmosphere to reflow the solder, thereby forming a good solder joint between the source bridge and the metal heatsink. While the chip is in the furnace, a small weight is used to push it into the solder and assure proper wetting of the entire source-bridge area.

After the source bridge is bonded, ribbons are attached to the gate and drain pads. These ribbons are then connected to external matching circuits. Once the via chip is flipped, the gate and drain pads are readily accessible so that the matching network can be reworked. If a ribbon loosens from the device it can be rewelded or replaced. When a ribbon detaches from a conventional flip-chip device (without vias), the device is lost because all pads are under the chip and cannot be reached.

Performance

The first via devices were evaluated in the 8- to 18-GHz frequency range. These preliminary devices had 5- to 6-V pinchoff voltages. The gate-to-source reverse breakdown voltage was nominally 9 V at a 20-μA leakage current. The FET drain saturation current was 333 mA/mm, the transconductance 40 mS/mm, and the nominal gate length 0.8 μm. Three different device cell widths (0.15, 0.30, and 0.6 mm) are available on this mask set. The majority of the evaluation was performed on 0.6-mm-width devices at 12 and 15 GHz.

These devices typically exhibited a maximum unilateral gain (MUG) of 8 dB at 12 GHz and 6 dB at 18 GHz. Power test data are summarized in Table 2. Single-cell 0.6-mm devices were tuned and tested at discrete frequencies in the 8- to 18-GHz band with external double slug tuners (no internal tuning elements). The input and output standoffs were 0.1-pF capacitors. At 12 GHz, a single 0.6-mm cell had an output power of 271 mW with 4.3-dB gain and 25% power-added efficiency. This device, with internal lumped-element matching, had an output power of 308 mW with 4.5-dB gain and 28% power-added efficiency. When the device was optimized for efficiency, an output power of 231 mW with 5.2-dB gain and 31% efficiency was measured. At 15 GHz, a lumped-element matched and combined two-cell device had an output power of 448 mW with 4.0-dB gain and 19.7% efficiency. The results are very encouraging.

Table 2—Large-Signal Results for Flip-Chip Via GaAs FETs

Performance*	Frequency (GHz)						
	8	10	12	14	15	16	18
A. Single-(0.6-mm)Cell Via Device (No Matching)							
Output Power (mW)	253	325	271	230		212	139
Power Gain (dB)	5.1	4.5	4.3	4.1		3.7	3.3
Efficiency (%)	29	26	25	20		17	6
B. Single-(0.6-mm)Cell Via Device (Lumped-Element Matched)							
Output Power (mW)			308 (231)				
Power Gain (dB)			4.5 (5.2)				
Efficiency (%)			28 (31)				
C. Two-Cell (0.6-mm/Cell) Via Device (Lumped-Element Matched and Combined)							
Output Power (mW)				450	448	350	
Power Gain (dB)				4.0	4.0	3.2	
Efficiency (%)				19.0	19.7	12.0	

* Parenthetical values (see under B.) show the amplifier tuned to maximum efficiency.

Conclusions

A new format has been developed in which the FET device and passive-circuit properties of monolithic circuits can be independently optimized. This format is a flip-chip device with gate and drain via connections to the back side of the substrate. Because the device-to-carrier thermal resistance, the source inductance, and the Q factor of the printed passive circuits are independent, each can be optimized for best performance. This circumvents a basic problem of conventional monolithic circuits with a source via format where all three variables are dependent on the substrate thickness.

GaAs power FETs were fabricated by a laser processing technique to form via connections through thick semi-insulating substrates. Vias with 12.5- to 75-μm diameters were demonstrated through substrates as thick as 0.350 mm. The experimental power devices fabricated were evaluated at frequencies up to 18 GHz and shown to be very promising. Efficiencies as high as 31% and an output power per unit device width of 0.5 W/mm were measured.

Potential applications for the laser-via technology and the flip-chip gate and drain-via format include circuits that must be mass produced and that require integration of the active and passive elements. These components include monolithic FET amplifiers, FETs with monolithic matching and combining networks, broadband distributed amplifiers, and even low-loss passive filters.

Acknowledgment

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Advances in the Design of Solid-State Power Amplifiers for Satellite Communications*

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Abstract—The development of solid-state power amplifiers (SSPAs) to replace traveling-wave-tube amplifiers in satellite communications systems is described. The initial development work, which began in the mid-1970s, was made possible by the development of the GaAs FET device. This early development work resulted in a significantly improved communication system; to date, over 100 SSPAs have been included in operating geosynchronous satellites. Operational results for these transponders indicate a significant improvement in channel capacity due in large part to the linearity achievable with SSPAs. In this paper, we discuss the design of and give test results for several advanced SSPAs designed to operate at higher output power (6, 10, and 12 W) than the earlier design.

Introduction

During the past several years, RCA has been involved in the development of solid-state amplifiers for communication satellites. Part of this involvement resulted in the development of a space-qualified 8.5-watt amplifier which was launched on the first all-solid-state C-band communication satellite, RCA Satcom 5, in Oct. 1982. Since that time, the design and development of several advanced solid-state C-band amplifiers has been completed.

The initial work focused not only on the rf performance of SSPAs, but also upon such aspects of amplifier design as producibility and

* Partial funding for this program has been provided by Intelsat under Contract INTEL-138.

reliability. These factors limit the choice of components available for the amplifier and also influence the mechanical and thermal designs. The preliminary design resulted in an amplifier that not only met the rf performance goals, but that could also be space-qualified.[1]

The amplifiers developed initially comprised a number of stages that featured both high-gain and linear amplification. The first stages, in a single-ended design, utilized low-noise FETs with their high associated gain. A temperature compensation network was incorporated in the gate-bias circuit of these stages to achieve gain stability over the operating temperature range of from +5 to +50°C. The next stages were linear amplifiers used to drive the power stages. These stages operate in the linear region of the FET device, thereby reducing the overall third-order intermodulation ratio. The last two stages were high-power FET amplifiers. The final output stage consisted of balanced amplifiers combined by interdigitated couplers. An output isolator was used, in addition to the interdigitated combiner, to ensure an output VSWR less than 1.25:1.

Amplifier Design

The work conducted under the advanced generation SSPA design program began with an extensive amplifier configuration study to determine the optimum design to provide higher power capabilities than the earlier SSPAs (i.e., 6.0 W, 10.0 W, and 12.0 W) while maintaining the overall performance and reliability advantages of the solid-state power amplifier. This study has resulted in amplifier designs that exceeded the required minimum rf output power, while improving such performance requirements as power-added efficiency and intermodulation distortion.

The amplifier configurations selected for the 6.0- and 12.0-W SSPAs were a one-driving-three design and a two-driving-six design, respectively. These designs, while nonbinary, are the optimum for achieving the overall performance goals. The capabilities of the 6.0-W design have been described elsewhere.[2]

The amplifier configuration selected for the 10.0-W amplifier is similar to that of the 8.5-W Satcom SSPA design. It utilizes a two-driving-four configuration in the high-power stages.

Block diagrams of the three SSPAs are shown in Fig. 1. Fig. 2 is a photo of the 12-watt SSPA showing the layout of the different stages.

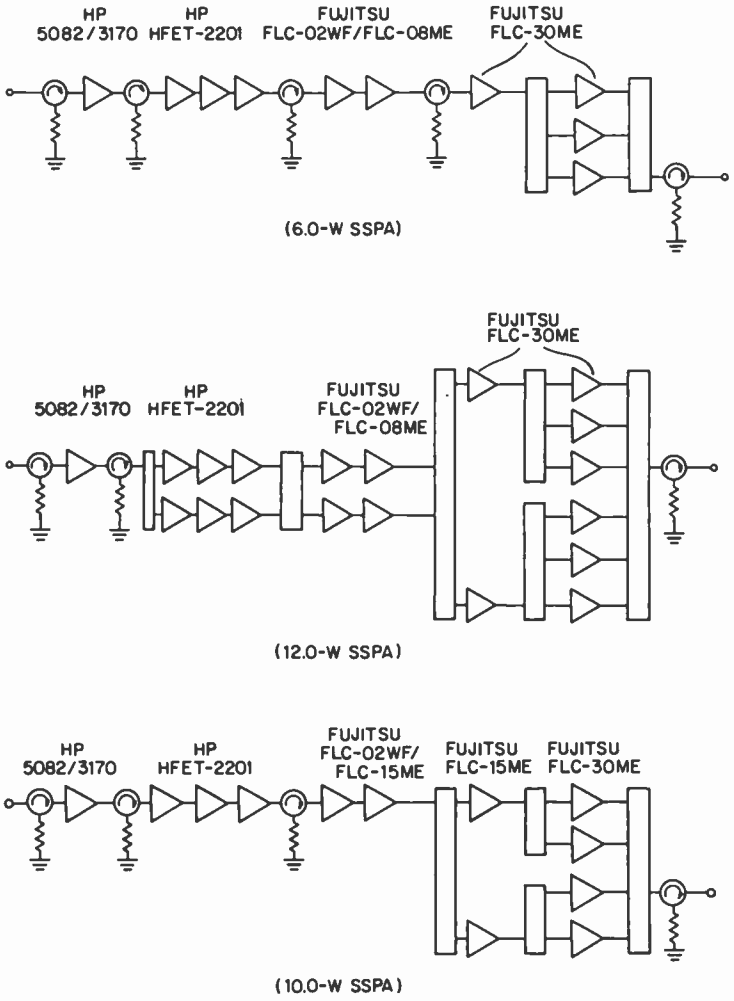

Fig. 1—Block diagram of 6-, 12-, and 10-W SSPAs.

Driver Amplifier

High-Gain Stages

The first stage of amplification in these SSPAs employs Hewlett-Packard HFET-2201 packaged FETs. The amplifier utilizes inter-stage-matching to reduce the size required for the high-gain stages. Previous SSPA designs used single-stage matching with 50-Ω input and output impedances and an isolator between stages. The design

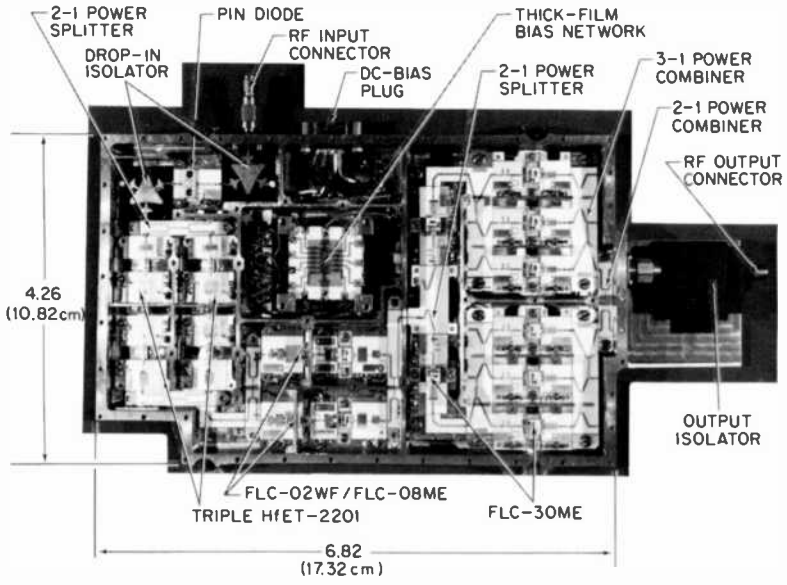

Fig. 2—12-Watt C-band SSPA.

of this amplifier demonstrates the advantage, from a size and weight perspective, of utilizing interstage-matching.

The requirement of increased gain necessitated the redesign of the high-gain stage. The goal was to provide 30-dB gain over the 3.7–4.2 GHz band width and to prevent oscillations in the HFET-2201 devices. Oscillations had been found to occur under some load and source conditions in the 3.5-GHz region. It was determined that the use of negative feedback could prevent these oscillations from occurring, and CAD modeling techniques were used to develop a feedback network. The use of feedback, however, reduced the available gain and it was necessary, therefore, to redesign the high-gain stage using three devices in cascade, with interstage matching, to achieve the required 30-dB gain. This new stage is smaller than the previous two-stage design. The effect of the added third device on the power-added efficiency of the overall SSPA is negligible due to the device's low dc requirements.

Linear Amplifier Stage

The second stage consists of linear amplifiers that have a gain of over 20 dB and an overall power-added efficiency greater than 22%

at an output power of more than 450 mW to drive the power stages. This linear amplifier stage utilizes interstage-matching, as does the high-gain stage, to minimize the size and weight of the overall integrated amplifier. Proper selection of devices for this stage was necessary to obtain the required output power without serious gain compression. The devices selected were Fujitsu FLC-02WF and FLC-08ME GaAs FETs. These devices are capable of providing output powers of 200 and 630 mW, respectively, at the 1-dB gain compression point while providing the required power-added efficiency at 4.0 GHz.

Power Stages

The high-power output stages for the three SSPAs are shown in the block diagrams in Fig. 1. All designs use balanced stages to achieve the required output power: the 6.0-W SSPA uses a one-driving-three configuration, the 10.0-W SSPA uses a two-driving-four configuration, and the 12.0-W SSPA uses a two-driving-six configuration. Design considerations for each of the amplifier stages are identical regardless of the configuration considered.

In these designs, a single-ended amplifier is used to drive the balanced amplifier stages. Each balanced stage consists of two or three transistor amplifier circuits combined by quadrature hybrids. The input power is split equally by the input hybrid, and the amplifier outputs are combined in the output hybrid. Based on the assumption that the FET amplifiers in each arm are reasonably similar, the input and output VSWRs are then determined by the couplers.

The design goals for the power stages were to achieve high rf output with high efficiency and good linearity. The first step in attaining this goal, as it is for the previous stages, is to measure the S parameters, plot the impedance, and then to design an initial input-matching circuit.

The next step, and the main difference between designing small- and large-signal circuits, is to characterize the device under large-signal input conditions. Since the output impedance of the device is a function of the input power, it is imperative to know the impedance variation exactly, in order to design an output-matching circuit that will provide the required output power.

The equipment used for large-signal modeling is a unique RCA development called automatic load pull.[3] The load-pull equipment presents a known output impedance to the device while simulta-

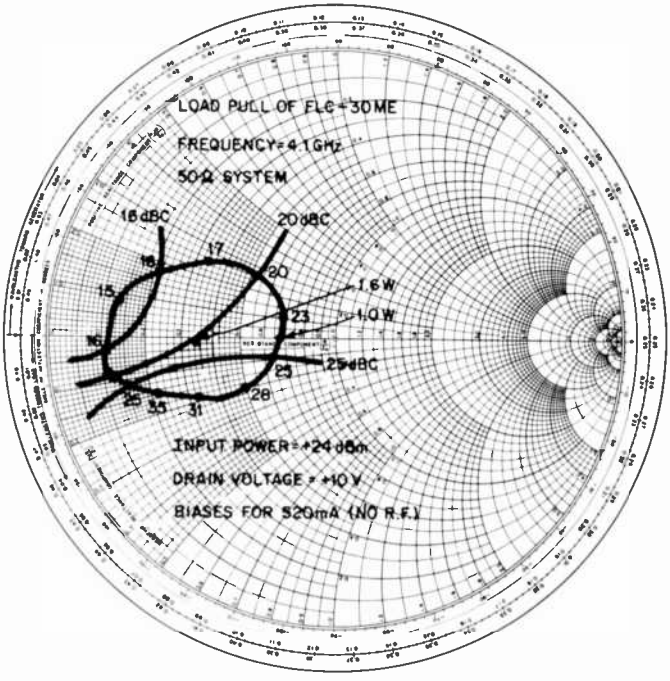

Fig. 3—Load-pull contour of the FLC-30ME device with IMD contours overlayed for 4.1 GHz.

neously monitoring the output power. The result is a plot of output power versus impedance.

Another unique use of the load pull is to plot the intermodulation distortion (IMD) of an amplifier stage as a function of the output-matching circuit impedance. By overlaying the power and IMD contours, the best output impedance can be selected. Fig. 3 shows the power and IMD overlay plots of the FLC-30ME at 4.1 GHz.

The last step is to realize the necessary output impedance over the full band. Once this is accomplished, the input match can be fine tuned using CAD techniques to give the best amplifier response.

Temperature Compensation

FET devices undergo an inherent reduction in rf gain as the temperature of the device increases. This gain change with temperature can be attributed to two changes in the active-layer properties: (1) carrier drift mobility decreases with temperature and (2) peak drift

velocity decreases with temperature. Both of these factors increase the amplifier gain below room temperature and decrease it above room temperature. Dynamic temperature compensation techniques have been developed to decrease these changes. Temperature compensation was initially used for single-gate amplifiers and recently has been adapted to dual-gate FET amplifiers.

To stabilize gain versus temperature to a first order, we must stabilize the drain current versus temperature. One method of doing this is to provide a dc feedback voltage of the proper polarity to the gate that pulls the drain current in the right direction. In the case of multistage high-power amplifiers, however, the gate bias of the power devices should not be varied with temperature, since that results in shifts in the device operating point which, in turn, results in additional performance variations (P_{out}, efficiency, and IMD). Therefore, it is necessary to compensate the amplifier performance by controlling only the gate bias of the high-gain *input stages*.

A few problems arise when the above technique is used. The "swing" in gate voltage that is needed is rather large. To realize a thermistor network that would accommodate this large swing is extremely difficult if not impossible. Another problem that occurs when large voltage swings are necessary is gain tilting. The gain response of an FET amplifier is very sensitive to changes in gate voltage. Therefore, the use of a gate-bias temperature-compensation network, to offset the effects of temperature on gain, may cause more problems than it solves.

In light of the above analysis, a second compensation method, a PIN diode attenuator, was chosen. To eliminate the large VSWR problem normally associated with diode attenuators, an isolator is used at the input and output of the attenuator cirucit. The PIN diode selected is the Hewlett-Packard 5082-3170. Fig. 4 shows test results obtained for this device using a Piezo Electric Products, Inc., thermistor 15TE2 as the temperature-sensitive element in the bias circuit. Fig. 4 also shows the expected change in overall gain of the SSPA.

Mechanical Design

Some considerations in the mechanical design of an SSPA are that it be lightweight (less than 1 lb), compact (20 in^3 or less), and readily constructed using assembly-line techniques, and have good mechanical interstage isolation and good thermoconductivity.

A modular concept was used in which the amplifiers are divided

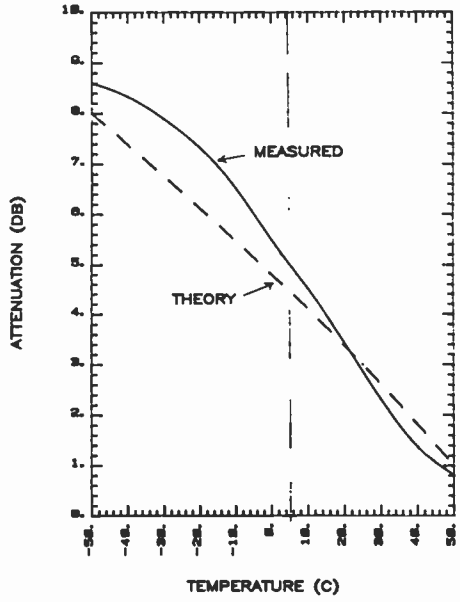

Fig. 4—Attenuation versus temperature using HP PIN diode 3170 as temperature-sensitive element in bias circuit.

into two subassembly stages, the driver stage and the power stage. Each has its own mounting plate. These stages are interlocked during integration to form the complete amplifier. Grounding is accomplished in the drive stage by soldering the Kovar pallets to the nickel-plated aluminum mounting plate by use of a low-temperature solder and then using screws to fasten each pallet. The power stage has cutouts in the mounting plate under the junction of each pallet, and grounding is accomplished by soldering a copper strap across each junction. All pallets are screwed to the mounting plate. Fig. 5 illustrates the mechanical design of the 6.0-W SSPA.

A three-step soldering technique was used for each pallet assembly. First, a high-temperature solder is used to attach the matching circuits to the pallet; second, an intermediate solder is used for all other components except the FET; and last, a low-temperature solder is used to solder in the FET. This technique allows rework and repair at the first two steps without any possible damage to the FET; it also allows removal of the FET without damage to the pallet assembly should the device have to be changed.

The rf interstage connections on the top side of the pallets are accomplished by using gold ribbon and by parallel gap-welding the

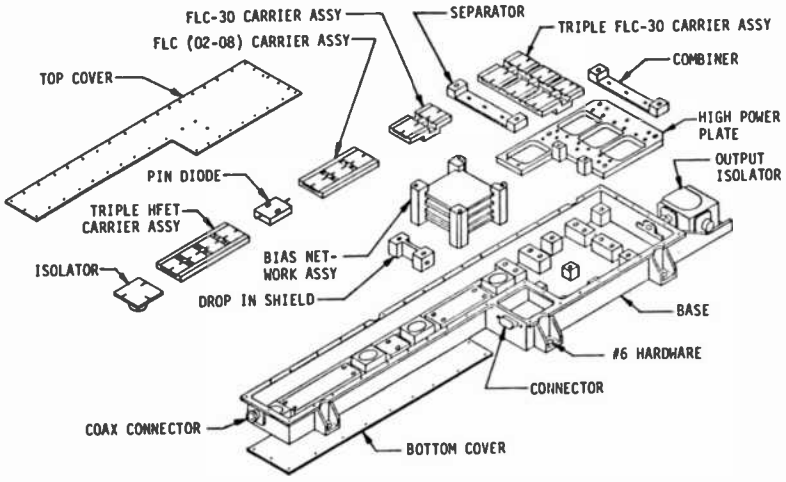

Fig. 5—Mechanical design of 6-W SSPA.

ribbon across the rf lines between the pallets. This method is used to minimize the amount of soldering to the gold-plated rf lines.

An additional advantage of the stepped soldering and modular design concept is that operators can be easily trained to assemble the amplifiers using production-line techniques. This factor is important because the amplifiers are to be made in large numbers.

Test and Evaluation

Table 1 summarizes performance characteristics for 6.0-, 10.0- and 12.0-W SSPAs developed under the Advanced C-Band SSPA Pro-

Table 1—Summary of RF Performance

Performance Characteristic	Solid-State Power Amplifiers		
	6.0-W	10.0-W	12.0-W
Minimum Output Power (W)	6.30	10.0	12.60
Gain at Minimum Output Power (W)	63.0	64.0	58.0
Small-Signal Gain (dB)	65.0	67.0	59.2
Level of IMD Relative to Carrier at Input Drive for reported output power (dBc)	17.2	14.8	14.8
Power-added Efficiency (%)	25.0*	28.5*	26.0
Weight (g)	382.2	393.1	499.1
Volume (cm^3)	285.1	276.2	367.7

* Includes 85% dc/dc Converter.

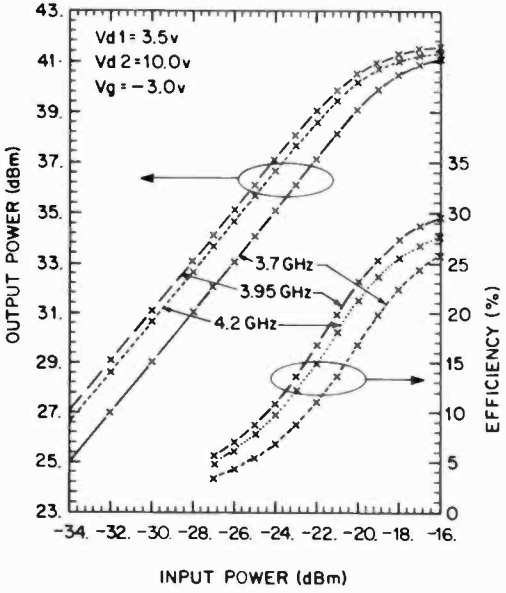

Fig. 6—Input power versus output power and power-added efficiency for the 12-W SSPA.

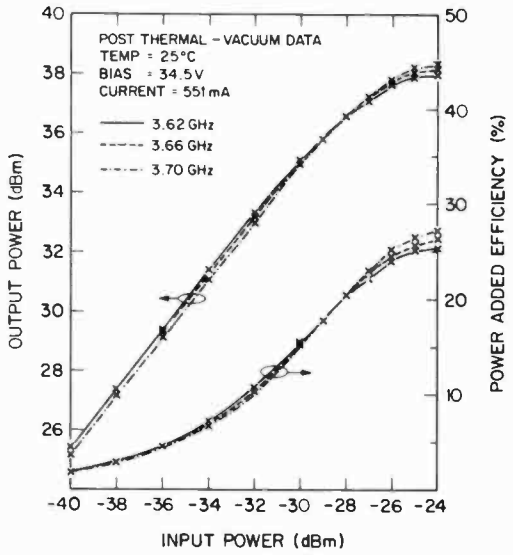

Fig. 7—Input power versus output power and power-added efficiency for the 6-W SSPA.

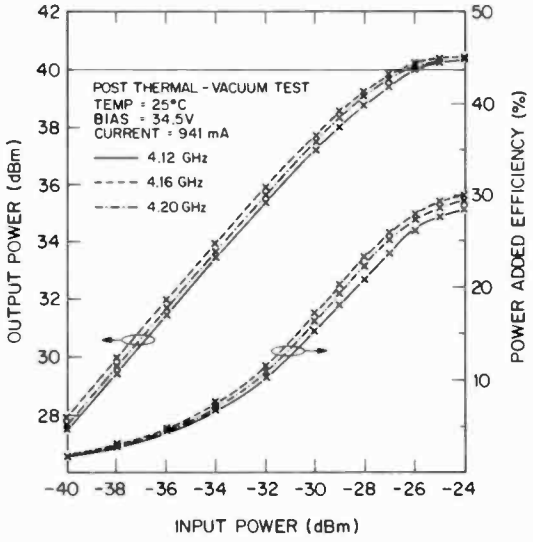

Fig. 8—Input power versus output power and power-added efficiency for the 10-W SSPA.

gram. This table gives worst-case data. It is believed that these test results are the best reported to date for SSPAs.

Fig. 6 shows an AM-to-AM transfer of the 12.0 watt SSPA operating across the full 3.7–4.2 GHz band. The data indicates a minimum small-signal gain of 59.2 dB at 3.7 GHz. The minimum output power of 12.60 watts also occurs at 3.7 GHz. Figs. 7 and 8 show test data for the 6.0- and 10.0-watt SSPAs, respectively, operating over channelized portions of the C-band down-link. The data in Fig. 7 for the 6.0-W SSPA operating over the 3.62–3.70 GHz band indicates a minimum output power of 6.3 watts (38.0 dBm) with a power-added efficiency of 25% at an input power of 0.003 mW (−25 dBm) at 3.62 GHz. Fig. 8 for the 10.0 watt SSPA operating over the 4.12–4.20 GHz band, indicates a minimum output power of 10.0 watts (40 dBm) with 28.5% power-added efficiency at an input power of −26.0 dBm.

The test results for the 6.0- and 10.0-W SSPAs were taken with a dc/dc converter. The converter supplies dc power to the SSPA from an unregulated dc supply (e.g., the satellite dc power buss). The dc-to-dc efficiency of the converter is a minimum of 85%, which means that the actual power-added efficiency of the 10.0-W SSPA is a minimum of 33.5% without the dc/dc converter.

Acknowledgment

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Communication Receivers for Satellites—A Review

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Abstract—This paper reports the development of all solid-state low-noise wideband receivers for use in communication and direct-broadcast satellites operating in the 5.9- to 6.4-GHz, 14.0- to 14.5-GHz, and 17.3- to 17.8-GHz uplink frequency bands. The receivers provide low-noise and spurious free down conversion of the uplink frequency bands to the downlink frequency bands of 3.7 to 4.2 GHz, 11.7 to 12.2 GHz, and 12.2 to 12.7 GHz, respectively, with excellent frequency stability. The receivers incorporate state-of-the-art GaAs FET devices and microwave integrated-circuit technologies. Details of the design and measured performance of receivers are given.

Introduction

Astro-Electronics has been designing and building communications satellites since the early 1970s, but not until 1978 did AE begin to design the microwave hardware used in the communication-system transponders. One of the first microwave subsystems to be designed and put into production is the 6/4-GHz communications receiver. This unit is a wide-bandwidth receiver covering the full communication spectrum assigned to the satellite, and it amplifies all of the signals of a transponder simultaneously. Since then, 14/12-GHz and 17/12-GHz communication receivers have also been developed and put into production.[1-3]

The 6/4-GHz receiver is used on C-band communication transponders. Its input band (uplink) is 5.925 to 6.425 GHz, and its output band (downlink) is 3.7 to 4.2 GHz. The 14/12-GHz receiver is used on the Ku-band commercial communication satellites. Its uplink is 14.0 to 14.5 GHz, and its downlink, 11.7 to 12.2 GHz. The

17/12-GHz receiver finds application on the direct-broadcast satellites. Its uplink band is 17.3 to 17.8 GHz and its downlink band, 12.2 to 12.7 GHz.

For the RCA Satcom and other communication satellites, all 12 channels of the transponder uplink are amplified and translated to the required downlink frequency band. Two transponders using the same frequency spectrum operate without mutual interference by cross polarization of the input and output signals; thus, two receivers operating continuously are required to provide 24-channel capacity. For the direct-broadcast satellites, no frequency reuse is presently planned. For the first satellite to be launched in 1986, only one receiver per spacecraft is operational at any one time. Descriptions and performance summaries of the 6/4-, 14/12-, and 17/12-GHz receivers are given in the following sections.

6/4-GHz Receiver

A block diagram of the 6/4-GHz receiver is shown in Fig. 1. Input signals are amplified at 6 GHz by a low-noise FET amplifier and then down-converted to 4 GHz by combination with the 2.225-GHz local oscillator in a diode double-balanced mixer. The resulting 4-GHz signal is then amplified to the required level by a four-stage FET amplifier. The stabilized voltage required by the amplifiers and local oscillator is produced by a power-regulator circuit that operates from the spacecraft's unregulated bus voltage. A photograph of the receiver is shown in Fig. 2.

The 6-GHz amplifier consists of two GaAs FET amplifier modules separated by ferrite isolators. The two-stage amplifier provides 24 dB of gain and a flat response across the 5.925- to 6.425-GHz band. Down conversion to the 4-GHz band is achieved in the mixer, which has isolators incorporated at all ports to minimize reflection on coaxial lines interconnecting modules. After mixing, a notch filter is provided to attenuate the second harmonic of the local oscillator at 4.450 GHz. The 4-GHz output from the mixer assembly is amplified by two FET amplifiers consisting of two transistors for each amplifier. The first amplifier provides 27 dB of gain over the 3.7- to 4.2-GHz band, while the second unit provides 25 dB of gain. These two 4-GHz amplifiers are similar in design, with isolators at the input and output of each transistor stage; however, the output stage of the second amplifier contains a medium-power FET to provide low intermodulation in output signals.

The 6-GHz FET amplifier is similar in design to the 4-GHz FET amplifier. It consists of input- and output-matching circuits in mi-

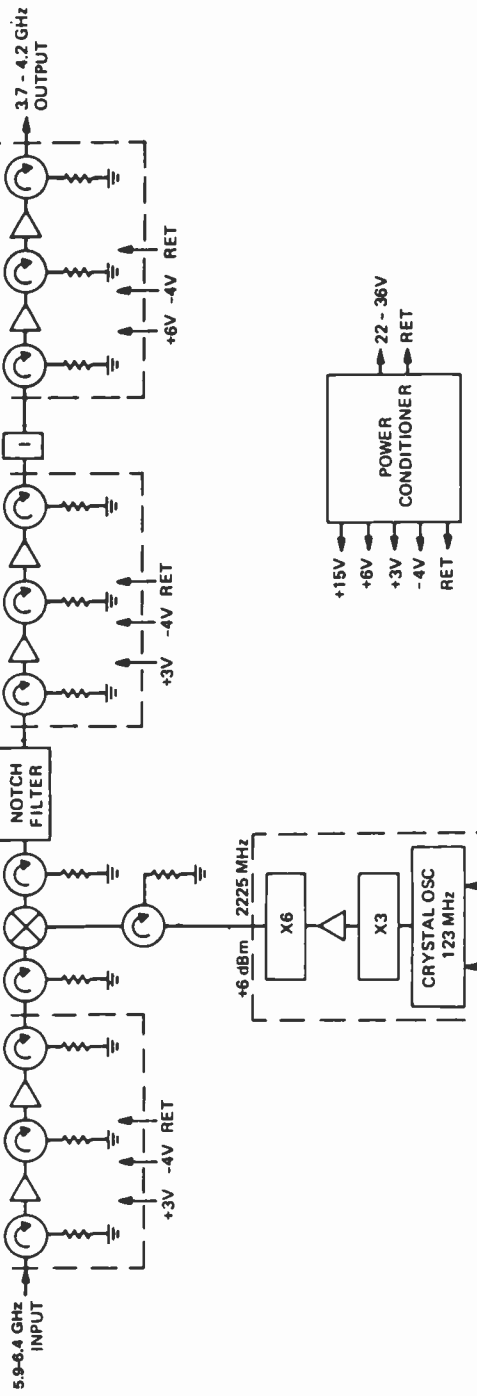

Fig. 1—Block diagram of 6/4-GHz receiver.

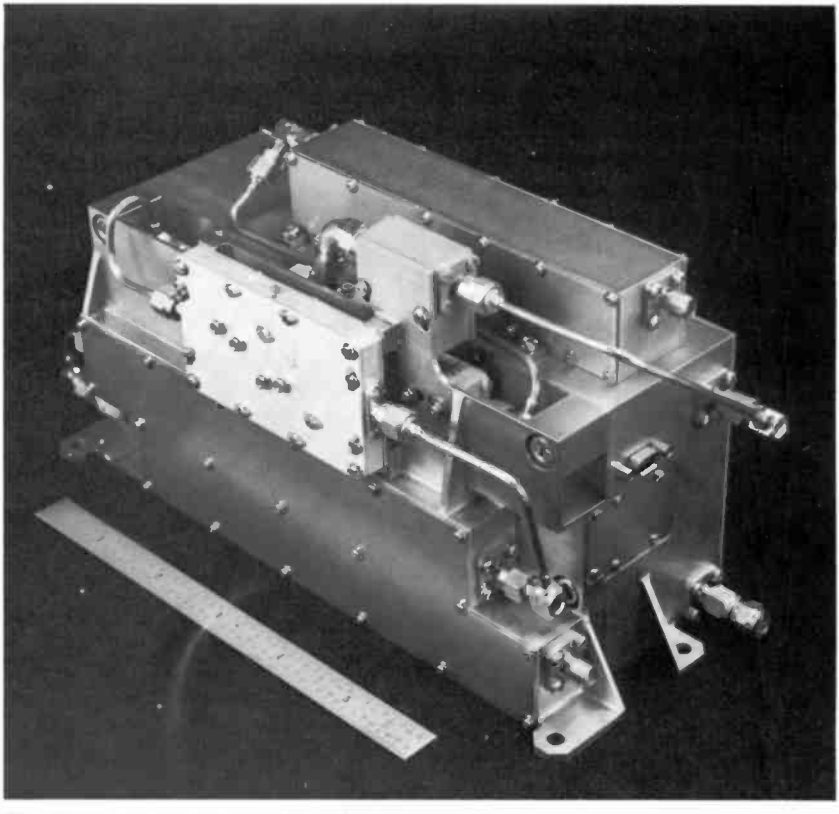

Fig. 2—Photograph of 6/4-GHz receiver assembly.

crostrip on 25-mil alumina to match the low impedance of the GaAs FET to 50 Ω. Matching networks were developed by means of RCA's COSMIC computer-aided design program. The matching network employed on both input and output is a two-stage Chebyshev quarter-wave transformer. Selection of transforming line lengths and impedance (width) is optimized by the computer to provide flat frequency response and the best impedance match across the full frequency band of the amplifier.

Interstage ferrite isolators are used at the input and output of each amplifier to achieve low input and output return loss and to prevent the input of the following stage from affecting the frequency response of each FET amplifier. The isolators are of drop-in type microstrip construction and are connected to the amplifier by welded gold ribbons. Fig. 3 shows the 6-GHz FET amplifier. The

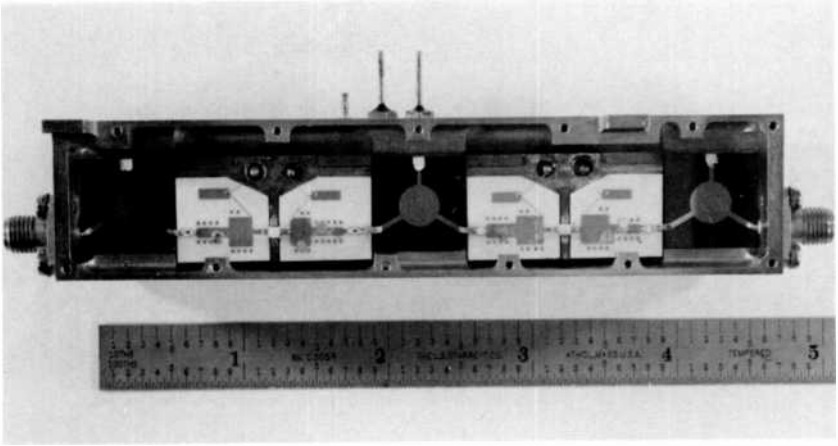

Fig. 3—Photograph of 6-GHz amplifier assembly.

two FET amplifiers with input- and output-matching networks on alumina substrates are mounted on Kovar* carriers and drop into the chassis; the isolators are soldered directly to the chassis.

The 6/4-GHz receiver operates over a temperature range of -7 to $+55$°C. The uncompensated FET amplifier will show a drop in gain at high temperatures and an increase in gain at low temperatures. To offset this effect and hold the gain constant, the current in the transistor can be increased at high temperatures, and decreased at low temperatures. This is done by varying the gate bias of each FET by means of a simple voltage-divider circuit containing a temperature-sensitive component and resistors. The temperature-sensitive component is a sensistor with a positive temperature coefficient that causes the FET current to increase at high temperatures and decrease at low temperatures. The resistors in the circuit set the gate voltage and linearize the temperature-compensating effect of the sensistor. By proper component selection, the uncompensated gain change can be reduced by a factor of 3 to 5, depending on transistor type and initial operating current.

The local oscillator consists of a crystal oscillator at 123.611 MHz, multipliers, amplifiers, and filters to generate a signal at 2.225 GHz. Each module is designed to work into a 50-Ω impedance and is tuned up and tested in test fixtures before assembly in the local oscillator housing, as shown in Fig. 4.

* Reg. trademark of Carpenter Steel. Kovar steel is an alloy having a thermal coefficient of expansion close to that of alumina.

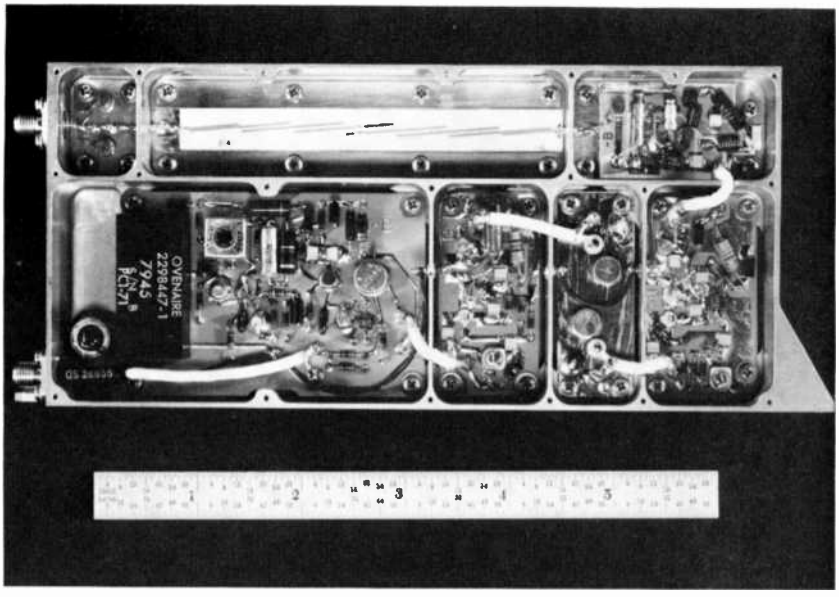

Fig. 4—Photograph of local-oscillator assembly (6/4-GHz receiver).

The output of the crystal oscillator is multiplied by three in a transistor and then amplified to a power level of +19 dBm at 370 MHz. This signal is then applied to a step-recovery diode to generate the sixth harmonic at 2.225 GHz. A microstrip bandpass filter and a lumped-constant lowpass filter are used to produce an output at 2.225 GHz, in which spurious signals are down at least 80 dB from the carrier.

The quartz crystal of the oscillator section is placed in a self-contained transistor/thermistor-controlled oven kept at 65 ±2°C. This results in a frequency drift of less than ±1 parts per million over the operating temperature of −7 to +55°C.

The mixer is a double-balanced diode design. It is optimized for inputs in the 5.925- to 6.425-GHz range and produces an intermediate frequency (IF) output at 3.7 to 4.2 GHz when used with a local-oscillator frequency at 2.225 GHz. The mixer is designed to operate with a local-oscillator input power level of +6 dBm and can be operated over the input range of +4 to +8 dBm with little change in the conversion loss of 6 dB. Isolators are placed at all three mixer ports to obtain low VSWR and to prevent reflections on signal lines that would introduce ripple in the passband of the receiver.

The notch filter is to reduce the level of the second harmonic (4.45 GHz) of the local oscillator, which is generated by the mixing process, by at least 30 dB. To this end, a two-pole filter is required. It consists of two quarter-wavelength resonators, short-circuited at one end and open-circuited at the other, that are proximity-coupled to the main transmission line.

Filter tuning is accomplished with capacitive-loading tuning screws located on the side covers of the filter. The tuning screws adjust the end-effect loading at the open end of the quarter-wavelength resonant lines, as well as the capacitive coupling between the resonant lines and the main transmission line. The center frequency of the notch is tuned to 4.448 GHz (12 MHz below 4.450 GHz) to account for a frequency shift when the receiver is operated in a vacuum.

Test Results for the 6/4-GHz Receiver

Extensive testing is performed on each receiver to verify that it meets all performance specifications. Testing starts at the module level, with each FET module being tested to demonstrate gain and flat response across the band and in the temperature range of -7 to $+55$°C. Modules are then placed in a chassis, tuned, and retested at the subassembly level.

The same testing process is repeated on the local-oscillator printed-circuit boards so that each is aligned in a test fixture. After all subassemblies are tested, they are assembled into the receiver chassis; the completed receiver FET amplifiers are then fine tuned with gold tabs on the alumina substrate to equalize the gain so that variations in gain across the 500-MHz band are no more than about 0.5 dB. Receiver gain is set to 60 dB by placing a fixed attenuator pad into the 4-GHz FET amplifier chain. A series of temperature tests are performed to measure gain at hot and cold temperatures. Fig. 5 shows the gain of a typical receiver at -7, $+27$, and $+45$°C, in which the gain-adjust attenuator pad had been selected to put the receiver gain in the range of 59 to 61 dB over the temperature range. A receiver-noise figure of 3.0 dB is typical at ambient temperature across the 500-MHz frequency band. At $+45$°C an increase of 0.2 dB in the noise figure can be expected.

In addition to the bench and thermal tests, the receiver is subjected to vibration in three planes and to several days of operation in a thermal vacuum to verify performance in a simulated space environment.

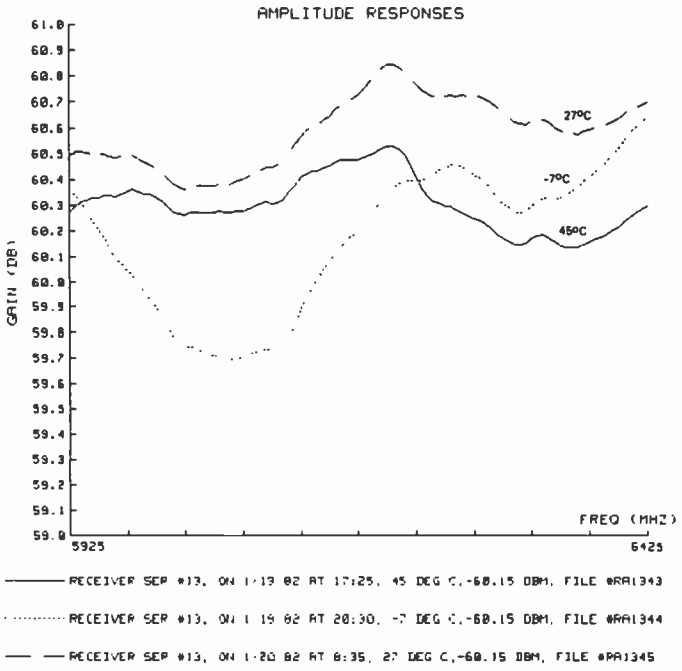

Fig. 5—Amplitude response of a flight 6/4-GHz receiver.

14/12-GHz Receiver

As the communication satellite allocations at C-band have become filled, the industry's attention has shifted to Ku-band frequencies (14 to 14.5 GHz uplink and 11.7 to 12.2 GHz downlink). Astro-Electronics has developed an all-FET Ku-band receiver for use on Ku-band spacecraft, starting with the launch of Spacenet 1 and 2 in 1984. A block diagram of this receiver is shown in Fig. 6, and a performance summary is listed in Table 1. The receiver is similar in design to the C-band unit except that the low-noise FET amplifier is now at 14 GHz and the output is at 12 GHz. A close look at the Ku-band design shows that the FET amplifiers consist of two transistors that form a basic gain block or module. These two transistor modules are then cascaded with isolators at the input and output. This technique reduces the size of a two-transistor amplifier by eliminating the interstage isolator and combining the output-matching network with the input-matching network of the next stage. A photograph of the Spacenet receiver is shown in Fig. 7.

A typical two-stage amplifier at 14 GHz containing Nippon Elec-

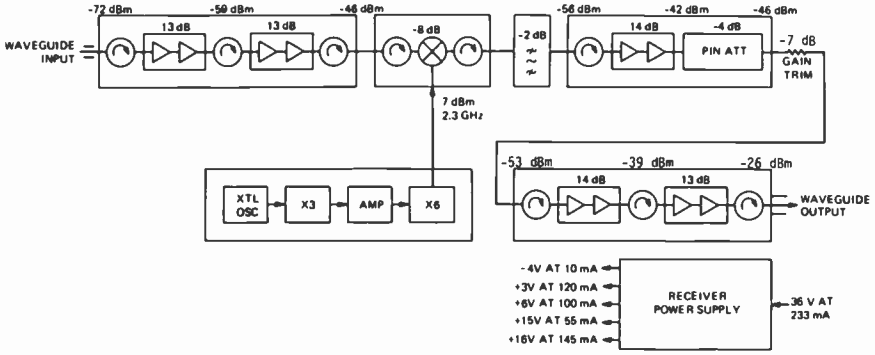

Fig. 6—Block diagram of 14/12-GHz receiver.

tric's NE13783 transistors has 14 dB of gain and a 3-dB noise figure. When two such units are combined in an amplifier chassis (shown in Fig. 8), the resulting amplifier has about 28 dB of gain and less than 0.5 dB of gain variation across the 14- to 14.5-GHz band. A microstrip isolator has not been used at the input to the 14-GHz amplifier because it would contribute to the loss and noise figure. Instead an iso-adapter, a waveguide-to-subminiature assembly (SMA) adaptor with a built-in isolator, is used because it adds only 0.25-dB input insertion loss and maintains an input VSWR of 1.15:1.

Designs of the 12-GHz FET amplifiers are similar to those of the 14-GHz units, except that the transistors used are Hewlett-Packard's HFET 2201 for small-signal stages, and a medium-power Fujitsu FLX03 FET is used in the output stage to provide low intermodulation distortion.

Fig. 9 shows a photograph of the 12-GHz FET amplifier. A p-i-n diode attenuator is included in this design after the first transistor pair so that the receiver gain can be adjusted to correct for decrease in gain from aging of the transistors. This p-i-n attenuator provides 3.5 dB of gain adjustment in 0.5-dB steps. An additional fixed attenuator pad is used to set the total receiver gain during alignment.

The mixer, a double-balanced microstrip design, is followed by a waveguide bandpass filter that attenuates the fifth and sixth harmonics of the local oscillator at 11.5 and 13.6 GHz. The local oscillator at 2.3 GHz is similar to that of the 6/4-GHz receiver except that the circuits are shifted from 2.225 to 2.3 GHz. This 3.4% shift in frequency is accommodated by the variable adjustments of the local-oscillator circuits without design modification.

Table 1—Receiver Performance Summary

Parameter	Satcom 6/4-GHz Receiver	Spacenet 14/12-GHz Receiver	DBS 17/12-GHz Receiver
Input/Output Frequency	5.9–6.4/3.7–4.2 GHz	14–14.5/11.7–12.2 GHz	17.3–17.8/12.2–12.7 GHz
LO Frequency	2.225 GHz	2.3 GHz	5.1 GHz
LO Stability	±1 ppm	±1 ppm	±1 ppm
Noise Figure	3.5 dB, max	4.8 dB, max	7.3 dB, max
Gain	60 ±1 dB	45.5 ±1 dB	35 ±0.5 dB
Gain Stability over Temperature	2 dB p-p	1.5 dB p-p	3.0 dB p-p
Gain Slope	0.02 dB/MHz, max	0.02 dB/MHz	0.02 dB/MHz
Group Delay	1 ns/36 MHz	2 ns/72 MHz	0.7 ns/24 MHz
3rd-Order Intercept Point	+28 dBm	+24 dBm	+25 dBm
Input/Output VSWR	1.2:1	1.15:1	1.15:1
Operating Temperature	−7 to 55°C	−5 to 50°C	−10 to 60°C
DC Power	8 W, max	8.4 W, max	9.0 W, max
Heater Power	——	6.6 W, max	——
Size	8.7 in. × 3.3 in. × 4.5 in.	7.75 in. × 4.62 in. × 5.75 in.	9.27 in. × 3.75 in. × 4.9 in.
Weight	3.25 lb	3.5 lb	3.5 lb

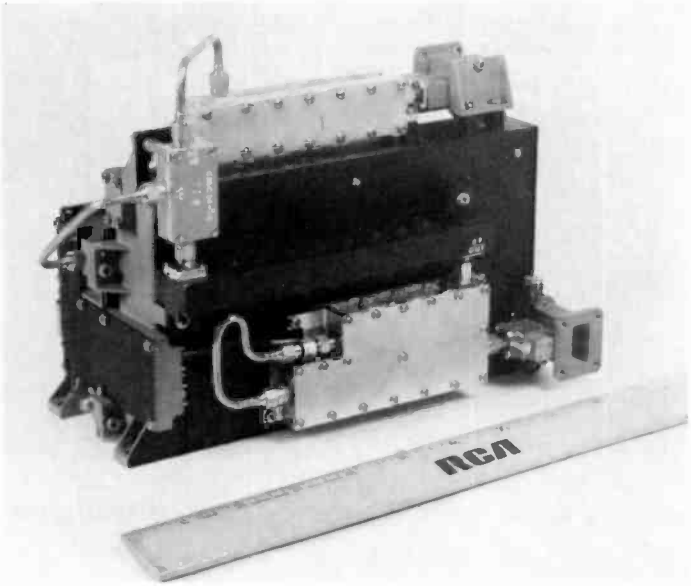

Fig. 7—Photograph of Spacenet 14/12-GHz receiver assembly.

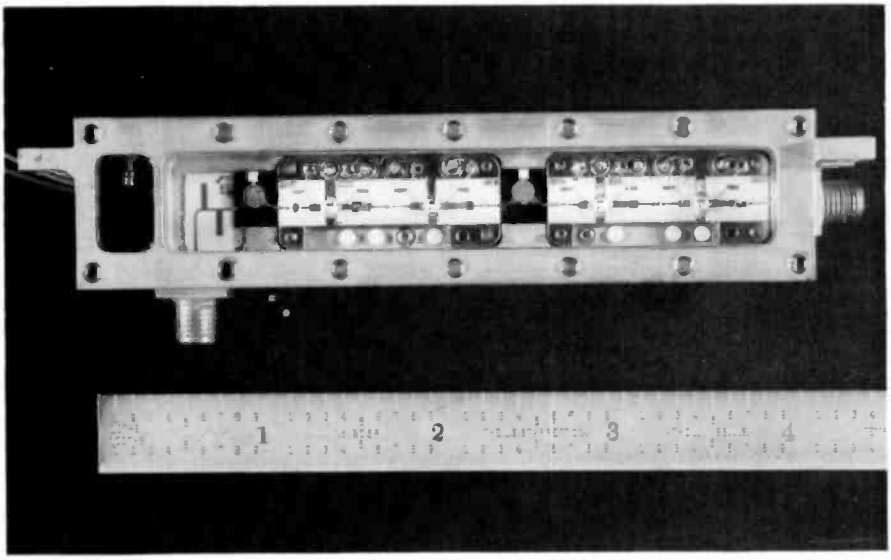

Fig. 8—Photograph of 14-GHz amplifier assembly.

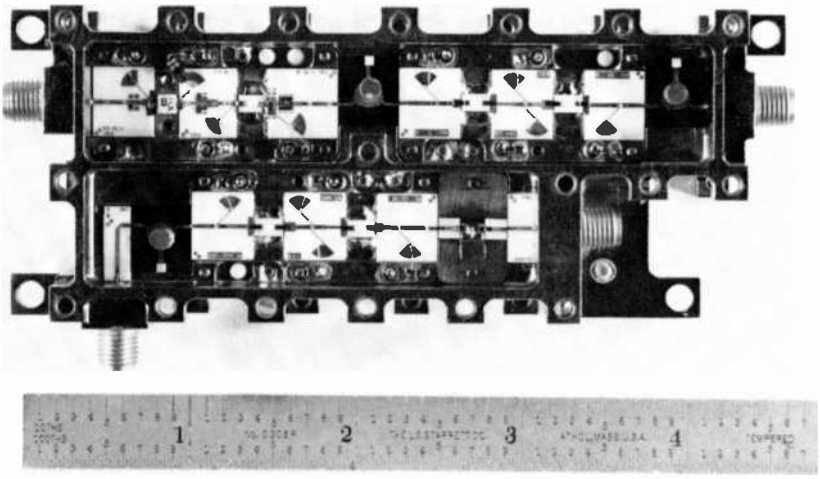

Fig. 9—Photograph of 12-GHz amplifier assembly (14/12-GHz receiver).

Test Results for the 14/12-GHz Receiver

A typical receiver frequency response is shown in Fig. 10. Slight retuning of the FET amplifiers was necessary to keep receiver gain variations to less than ±0.5 dB over the full 500-MHz band.

Flight performance specification for gain variations over operating temperature (0.8 dB peak-to-peak (p-p) for GSTAR and 1.0 dB p-p for American Satellite) required that heating elements be used on the 14- and 12-GHz FET amplifiers and the mixer to hold these units at a temperature of 30 to 32°C when the spacecraft environment is cold. A temperature sensor placed on the 12-GHz FETA controls heater power and keeps the FETA temperature from dropping below 30°C. To conserve power at the end of spacecraft life, heater power can be switched on and off by command.

Variations of the 14/12-GHz receiver have been made for the GSTAR and Satcom-K communication satellites. The GSTAR re-

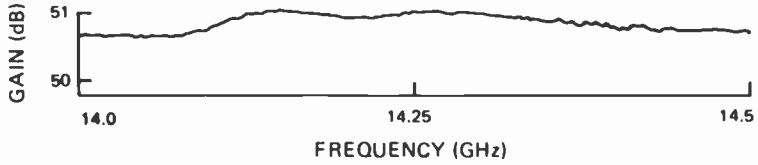

Fig. 10—Gain response of 14/12-GHz receiver.

ceiver incorporates an additional low-noise 14-GHz preamplifier to achieve a 3.4-dB noise figure and a 56-dB gain. For Satcom K the receiver has been coupled with a cooled low-noise amplifier (CLNA) to achieve a total receiver noise of less than 2.2 dB at 14 to 14.5 GHz. (The CLNA paper, by Busacca et al., is published in this issue of *RCA Review;* see p. 651.) The p-i-n diode attenuator and its decoder and controller were removed from the Satcom-K receiver, and the power supply for the CLNA was placed in this compartment. Performance characteristics for the Satcom-K receiver with CLNA are summarized in Table 2.

17/12-GHz Receiver

More recently, a 17/12-GHz receiver has been developed for use on the first U.S. direct-broadcast satellite (DBS) to be launched in 1986. This new type of satellite will employ high radiated-power carrier levels to provide television signals directly to private homes and businesses.

The communication receiver downconverts the 17.3- to 17.8-GHz uplink to 12.2- to 12.7-GHz downlink with excellent transmission characteristics of low noise, high linearity, high frequency stability, and low signal distortion.

A block diagram of the 17/12-GHz receiver is shown in Fig. 11. A photograph of the receiver assembly is shown in Fig. 12. The physical configuration of the 17/12-GHz receiver consists of the following three subassemblies:

- RF (or Microwave) Unit
- Local-Oscillator Unit
- DC/DC Converter Unit

Table 2—Satcom K 14/12-GHz Receiver with CLNA performance summary

Input/Output Frequency	14–14.5/11.7–12.2 GHz
LO Frequency	2.3 GHz
LO Stability over Temperature	±1 ppm
Noise Figure	2.2 dB, max
Gain	58 dB
Gain Stability over Temperature	1 dB p-p
Gain Slope	0.01 dB/MHz
Group Delay	0.5 ns/30 MHz
3rd-Order Intercept Point	+24 dBm
DC Power (CLNA, Receiver and Heaters)	20 W, max
Weight—Receiver	4.0 lb, max
Weight—CLNA	1.2 lb, max
Operating Temperature	−8 to 43°C
CLNA, Temperature	−35 to +25°C

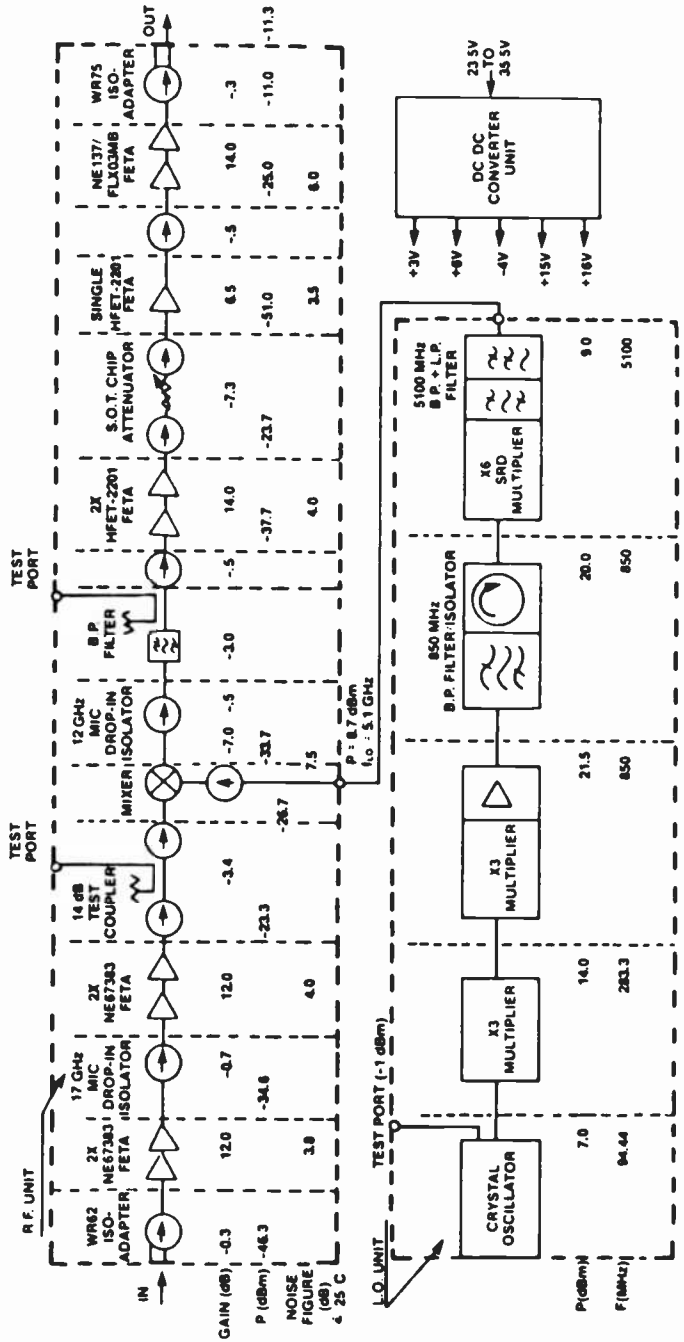

Fig. 11—Block diagram of 17/12-GHz receiver.

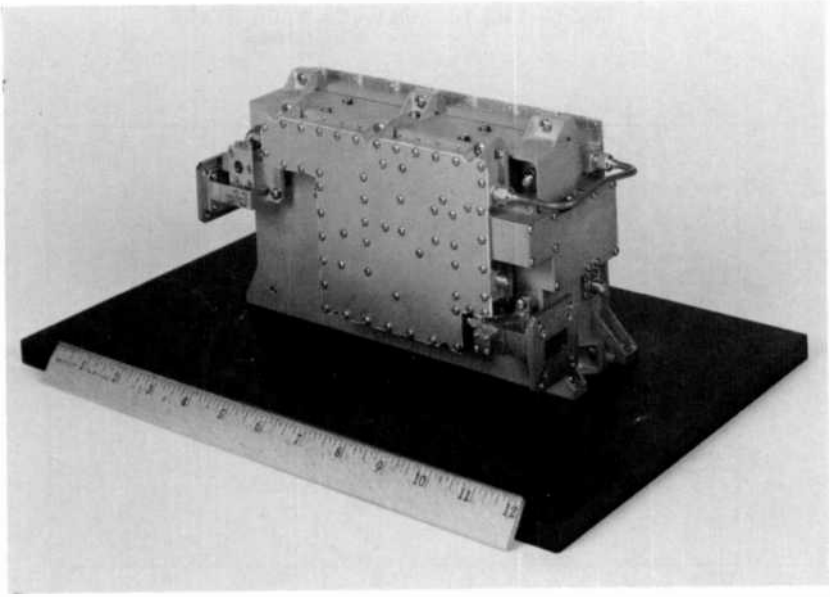

Fig. 12—Photograph of 17/12-GHz receiver assembly.

The three units are bolted together to form the receiver assembly. This design approach is similar to that used for 6/4-GHz and 14/12-GHz receivers and provides excellent rf shielding between the low-level microwave circuits and the high-level local oscillator (LO) and dc/dc converter circuits. It also makes it possible for the three units to be tested and assembled independently, allowing considerable flexibility in testing and high efficiency in production.

A block diagram of the rf unit (Fig. 11) shows that the 17-GHz input signals pass through a wideband iso-adaptor that provides a well-matched (VSWR $\leq$ 1.15:1) WR62 waveguide-to-coaxial(SMA) transition. The signals are coupled to a dual-stage NE67383 GaAs FET low-noise amplifier (LNA) via a coaxial(SMA)-to-microstrip launcher. The dual-stage amplifier has a noise figure of 3.8 dB and a nominal gain of 12.0 dB (at 25°C) to maintain the receiver noise figure. Fig. 13 shows the gain and noise-figure response of the 17-GHz dual-stage amplifier. The signals then pass through a wide-band 17-GHz microwave-integrated-circuit (MIC) drop-in isolator to a second dual-stage NE67383 FET low-noise amplifier, which is identical in design to the first dual-stage amplifier.

The dc decoupling networks on the gain and the drain bias ports of each dual-stage LNA are designed and optimized to provide at least 25-dB bandstop rejection in the image frequency band (7.1 to

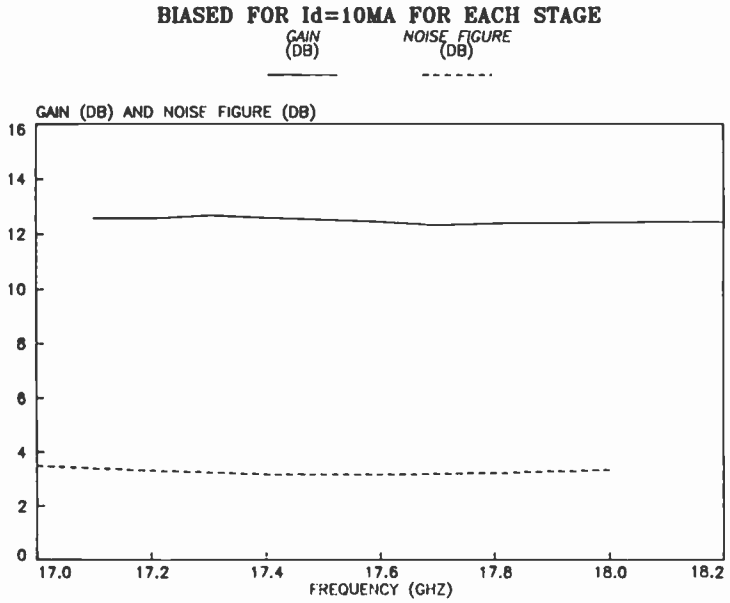

Fig. 13—Gain and noise-figure response of 17-GHz dual-stage low-noise amplifier.

7.6 GHz). Thus at least 50-dB image rejection is achieved by the two cascaded dual-stage amplifiers. This rejection is required to ensure negligible degradation of receiver noise figure due to contributions of the image frequency noise power. Fig. 14 shows the measured and computed wideband gain response of the dual-stage amplifier, including the image rejection response.

The amplified signals are passed through a 14-dB directional coupler located between two MIC isolators. The directional coupler provides a test port for the alignment of 17-GHz amplifiers. The main arm of the directional coupler feeds the signals into the rf port of a 17/12-GHz hermetically sealed drop-in double-balanced diode mixer. The LO port of the mixer is coupled to the local-oscillator unit via an interconnect substrate, a 5.1-GHz drop-in isolator and a semi-rigid coaxial cable. The IF port of the mixer feeds the down-converted 12-GHz signals into a 12-GHz coupled-line MIC bandpass filter via a 12-GHz drop-in MIC isolator. The filter is a seven-section, 0.01-dB ripple Chebyshev design and provides attenuation to the local-oscillator 2nd-, 3rd-, and higher-order harmonics and other unwanted mixing products. A 12-GHz 14-dB directional coupler follows the filter and provides a test port for aligning the 17-GHz amplifiers, mixer, and filter interconnections.

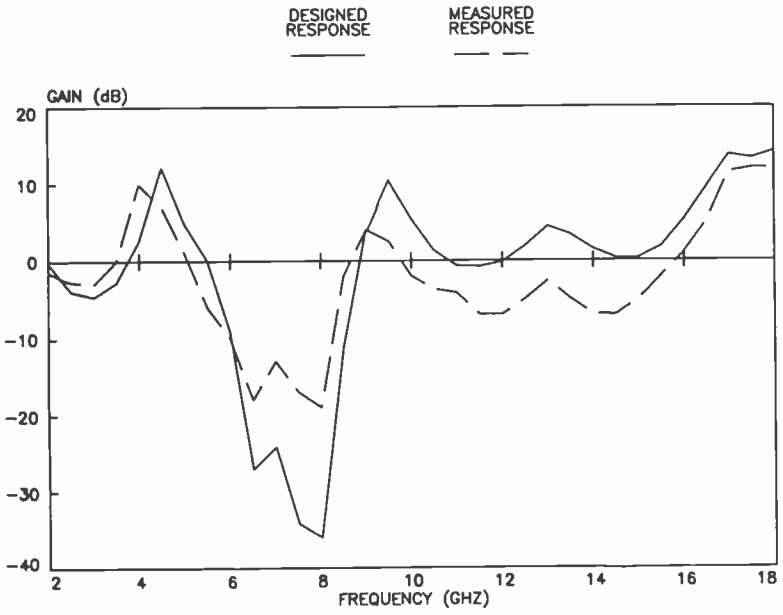

Fig. 14—Wideband gain response: 17-GHz dual-stage LNA.

The 12-GHz signals are then amplified by a dual-stage HFET-2201 GaAs FET amplifier that has a noise figure of 4.0 dB maximum and a nominal gain of 14.0 dB. A level-set chip attenuator reduces the signal levels to set the nominal gain of the receiver to 35 dB. The signals are then amplified in a single-stage HFET-2201 amplifier and an output dual-stage amplifier; the latter uses an NE13783 GaAs FET to drive a FLX03MB medium-power GaAs FET. The output dual-stage amplifier provides an overall third-order intercept point of 25 dBm (minimum) for the receiver. Finally, the 12-GHz signals exit the rf unit via a WR75 waveguide isoadaptor that has an output of VSWR $\leq$1.15:1. Drop-in ferrite isolators are used between various microwave modules to achieve good match and high isolation, resulting in a ripplefree gain response. Fig. 15 shows a photograph of the layout of the microwave circuit modules inside the rf unit housing.

The block diagram of the 17/12-GHz received (Fig. 11) also shows that the local-oscillator unit consists of a crystal oscillator at 94.44 MHz, followed by a $\times 3$, $\times 3$, $\times 6$ multiplier chain to achieve a 5100-MHz output frequency. The 94.44-MHz crystal oscillator is a Colpitts design, containing a fifth-overtone series-resonant quartz crystal placed in a proportional oven for achieving high-frequency

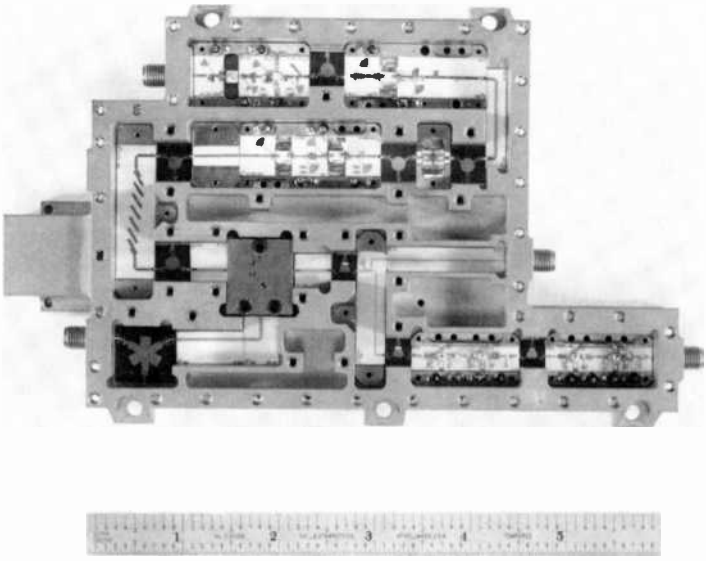

Fig. 15—Photograph of the rf unit (17/12-GHz receiver).

stability over life and temperature. The first ×3 multiplier uses a bipolar-transistor biased Class A but overdriven to form square-wave signals at its output. A double-tuned circuit in the collector provides the load impedance at the third harmonic (283.3 MHz) for power transfer and attenuates the unwanted harmonics. The multiplier has a saturated output power of 14 dBm and drives a second ×3 multiplier that is similarly designed. The second ×3 multiplier feeds the output at 850 MHz into a tuned amplifier that provides saturated output of 21.5 dBm. The amplified output is then filtered by a four-section 850-MHz combline bandpass filter to suppress the unwanted harmonics. A low-loss isolator couples the signal into a ×6 step-recovery diode (SRD) multiplier. The SRD multiplier provides an output of 11.5 dBm at 5.1 GHz. A MIC bandpass/low-pass filter combination follows the ×6 multiplier. The filters reject the unwanted harmonics of 850 MHz to provide a clean 5.1-GHz signal with an output power level of 9 dBm at the LO output port. All of the LO circuits are housed inside a compact housing. Fig. 16 shows the layout of the rf circuits inside the local-oscillator unit.

Test Results for the 17/12-GHz Receiver

A development model receiver was integrated, aligned, and tested

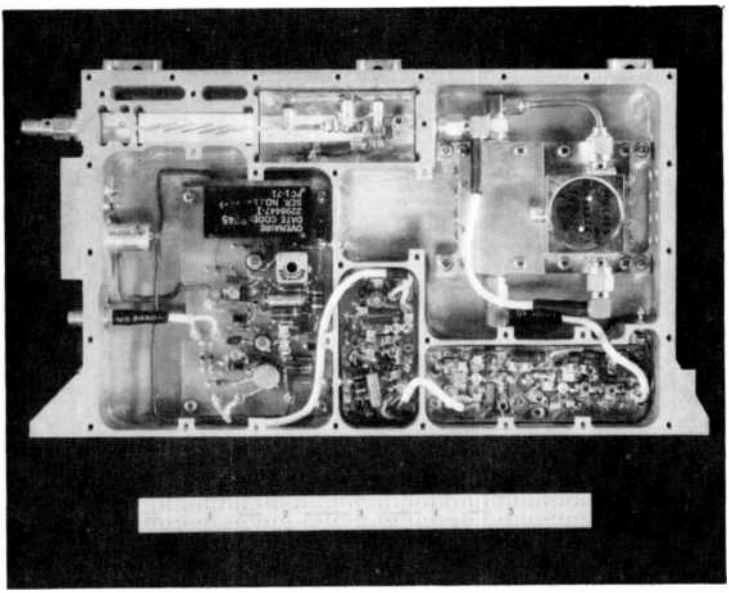

Fig. 16—Photograph of the local-oscillator unit (17/12-GHz receiver).

at ambient temperature and in thermal vacuum over a qualification temperature range of −10 to 60°C. Table 1 summarizes the specified performance of the receiver. Fig. 17 shows the measured gain and noise-figure data at −10, 25, and 60°C in a thermal vacuum. The receiver was successfully tested for electromagnetic compatibility and electromagnetic interference performance, such as conducted and radiated susceptibility, radiated emissions, and simulated spacecraft power-bus transients.

To prove mechanical integrity, the receiver was vibrated in all three axes (sine and random) up to 20 *g*'s. Postvibration and previbration measurements of gain and noise-figure response were in close agreement.

Conclusion

The design and measured performance of 6/4-GHz, 14/12-GHz, and 17/12-GHz communication receivers for the communication and direct-broadcast satellites have been presented. Performance measurements indicate that these receivers offer excellent transmission characteristics and stable performance in a spacelike operating environment. Flight receivers of identical configuration and design are being successfully manufactured at RCA Astro-Electronics for the various satellite programs such as Spacenet, GSTAR, American

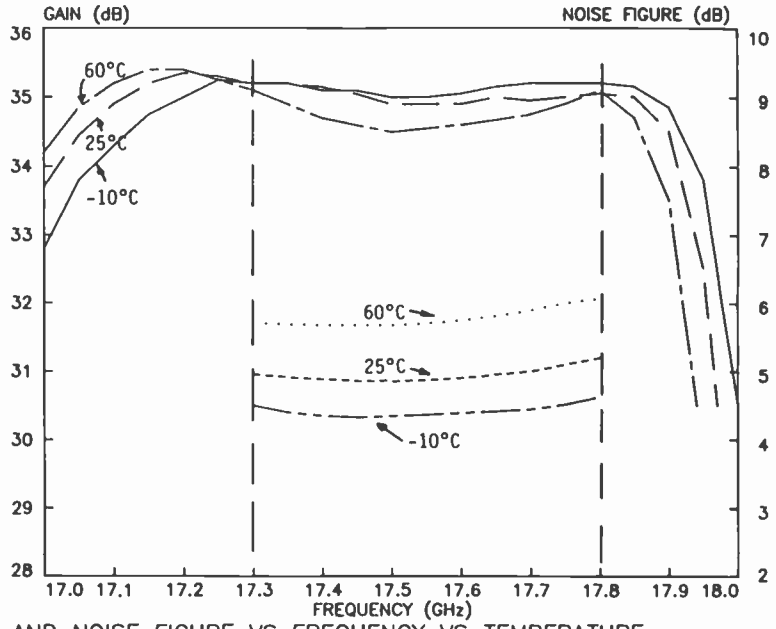

Fig. 17—Gain and noise-figure response of the 17/12-GHz receiver in thermal vacuum.

Satellite, RCA C-band and K-band Satcom, and Satellite Television Corporation's DBS.

Acknowledgments

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[2] S. S. Dhillon, P. Goldgeier, R. Sudarsanam, and H. Goldberg, "17/12 GHz Communication Receiver for Direct Broadcast Satellites," *Microwave J.* **27**(10), 107 (Oct. 1984).
[3] S. S. Dhillon, P. Goldgeier, R. Sudarsanam, and H. Goldberg, "17/12 GHz Communication Receiver for Direct Broadcast Satellites," *1984 IEEE MTT-S Int. Microwave Symp. Dig.*, May 30–June 1, 1984, San Francisco, CA, p. 257.

A 14-GHz Cooled Low-Noise GaAs FET Amplifier for Communication Satellite Application

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Abstract—Low-Noise parametric amplifiers have been used in satellite transponders operating at Ku band to produce overall system noise of less than 2.2 dB. Recent advances in GaAs FETs have made it feasible to produce amplifiers using these devices with performance levels approaching those of parametric amplifiers. To achieve the required low noise levels, the GaAs FETs must be cooled. A 14-GHz cooled low-noise amplifier (CLNA) is described, whose design is based on compromises between electrical, thermal, and mechanical design principles. Electrical design consisted of rf and power-supply development. RF design involved characterizing and matching GaAs FETs, and cooling required a power supply for the cooler (thermoelectric Peltier junction device) that maintains the amplifier at −50°C. Thermal design consisted of characterizing the heat load of the amplifier, specifying the cooler, and determining an appropriate location on the spacecraft. The mechanical design consisted of developing structural components that are compatible with the mechanical, thermal, and rf environments. Plastic waveguides were developed that serve as low-loss rf transmission mediums and thermal isolators. The engineering model described in this paper has a maximum noise figure, when cooled, of 2.1 dB, a minimum gain of 15.0 dB, and required 5.0 W of dc power to maintain this performance.

Introduction

Communication satellite transponders must be capable of sensitive signal detection because of the large amount of attenuation present in the uplink path to geosynchronous orbits. Ultralow-noise am-

plifiers are used on the front end of these transponders to establish the required sensitivity. Parametric amplifiers have previously been used at Ku band to achieve transponder noise figures of less than 2.2 dB.[1] Parametric amplifiers are sensitive and complex devices, however, and are difficult to adapt to the spacecraft environment.

Recent advances in the field of GaAs MESFET technology[2] have led to the production of GaAs FET amplifiers with noise figures approaching those of parametric amplifiers. The major noise contribution of a GaAs MESFET is thermal in nature.[3] Reducing the temperature of the FET will reduce the noise contribution and hence lower the noise figure of the amplifier. A cooled low-noise FET amplifier (CLNA) will produce noise figures equal to those obtainable with a parametric amplifier. CLNAs have been developed that use a variety of cooling methods and attempt to achieve cryogenic or near cryogenic temperatures.[4–7] Improvements in FET performance have made it feasible to produce a CLNA in a spacecraft environment without having to attain cryogenic temperatures. This paper describes the development of a CLNA that is used as the front end of a communication satellite transponder to achieve a noise figure of less than 2.2 dB.

Design Approach

The objective of this program was to design a cooled low-noise amplifier in the frequency range of 14.0 to 14.5 GHz that when used in conjunction with the 14/12-GHz communication receiver, would provide an overall system noise figure of less than 2.2 dB. The CLNA is to be separately packaged and compatible with the spacecraft environment. The performance parameters for the CLNA are as follows:

Frequency:	14.0–14.5 GHz
Gain minimum:	14.0 dB
Noise figure maximum:	2.1 dB
Input/output VSWR:	1.15:1
Power Consumption:	12 W
Cooler Power:	8W

Designing the CLNA was an integrated process that involved making trade-offs between the three design disciplines involved; electrical, thermal, and mechanical. A block diagram of the CLNA is shown in Fig. 1. To achieve the lowest noise figure, insertion losses on the input of the amplifier were minimized and the tran-

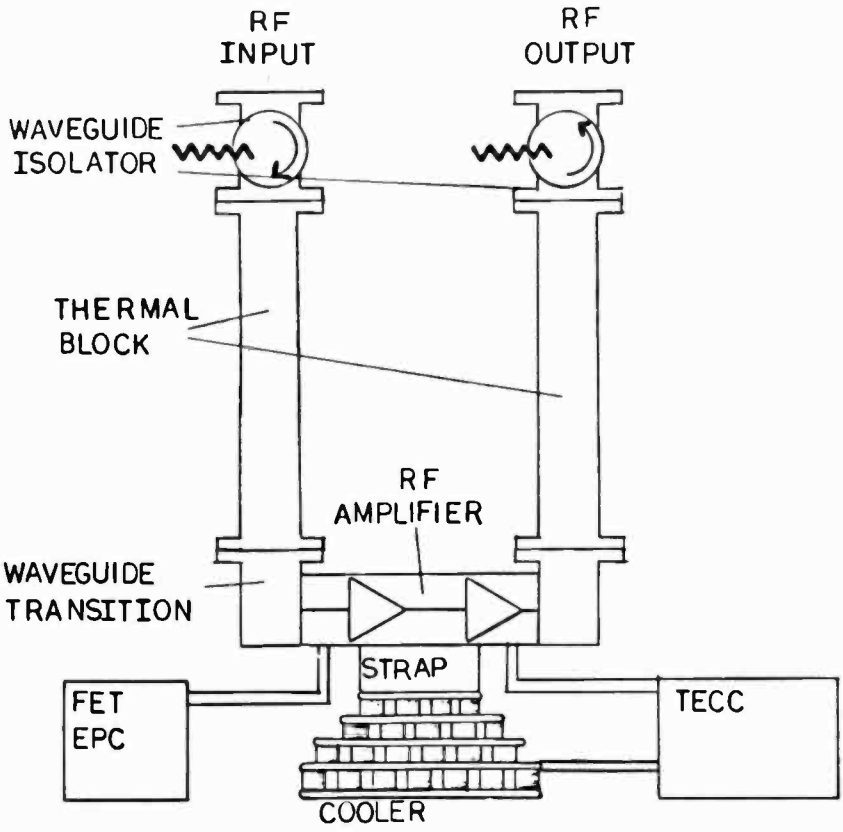

Fig. 1—Block diagram of cooled low-noise amplifier.

sistors were matched for minimum noise figure. Waveguide components were used for the rf input and output because of their low-loss characteristics. An rf transmission medium/thermal insulator was developed to serve as a low-loss rf input and to provide thermal conduction insulation. The amplifier required two stages of amplification. The FETs used in the amplifier were characterized for noise performance.

The cooling method selected was a thermoelectric Peltier junction device consisting of four stages of cooling. A flexible interface between the cooler and the amplifier housing was developed that allows for thermal stress relief and provides a low thermal resistance path. Since material selection was critical, because of the extreme operating temperature, an investigation of material properties was conducted. The amplifier housing was made as small as possible in

order to reduce the amount of heat that must be removed from the amplifier to achieve the desired operating temperature.

RF Design

The rf design consisted of four main tasks: a device survey, device characterization, amplifier design, and the development of an rf transmission line/thermal insulator (thermal block). The device survey consisted of an analysis of the available GaAs MESFETs based on low-noise-device specifications from various manufacturers. The NEC device NE67383 was selected as the most suitable because it has a nominal noise-figure specification that is at least 0.2 dB better than other devices.

The purpose of the device characterization was to determine the minimum noise figure (NF) and the optimum source impedance for minimum noise figure (Γ_{opt}). These parameters were determined by first taking direct measurements of the device, and then employing computer analysis to de-embed the actual values from the measurement results. NF and Γ_{opt} were then determined by a computerized convergence to the point of inflection on the parabolic relationship of NF and Γ_{opt}.[8]

The characterization required mounting the device in a test fixture, as shown in Fig. 2, consisting of input and output microstrip substrates and coax-to-microstrip launchers. The test setup, shown in Fig. 3, consists of the test figure, stub tuners, and bias tees along with the measurement equipment.

The tuners were adjusted to present different impedances to the device, and the noise figures, gains, and tuner positions were recorded. The *s* parameters of the tuning elements were measured on an automatic network analyzer from reference point PTa in Fig. 3.

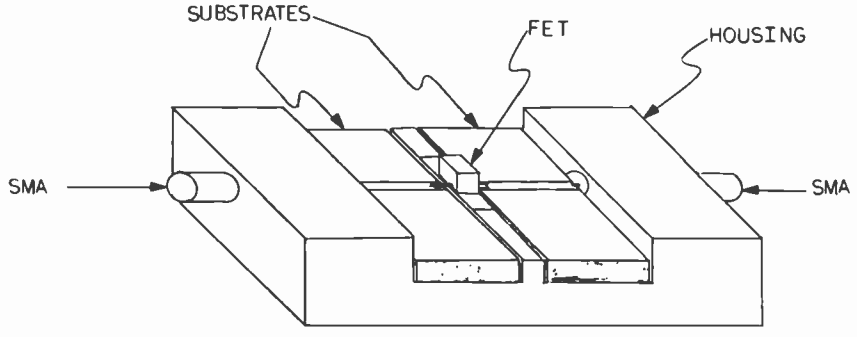

Fig. 2—Transistor test fixture.

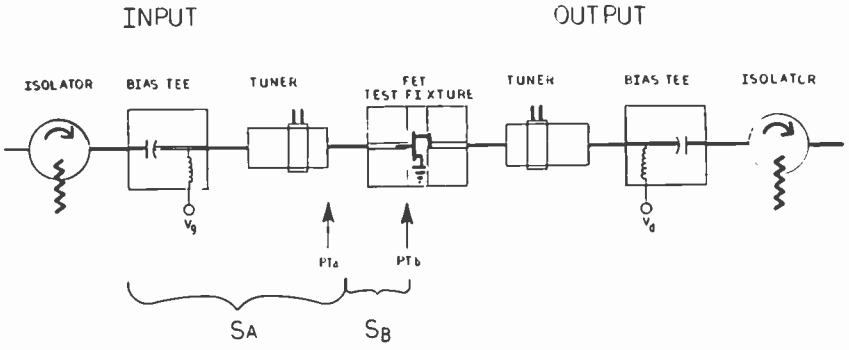

Fig. 3—Transistor characterization test setup.

To achieve an accurate *s* parameter measurement (i.e., referenced to the device leads, point PTb), the influences of the test fixture must be determined and removed. This correction was made by treating the test fixture and the rest of the test setup as separate components with individual *s* parameter matrices (see Fig. 3). The matrices were then cascaded and the impedances as seen by the device determined by computer model. The test fixture matrix was created through the use of the TSD (through, short, delay) characterization method.[9]

Another error introduced by the measurement technique is the insertion loss that is added to the noise figure measurement by the tuners, bias tees, and the test fixture. This error was compensated for by cascading the *s* parameters of the input matching network, determining the inverse gain (noise factor), and subtracting that value from the noise figure measurement.[10] The results of the characterization and the convergence of NF and Γ_{opt} are given in Table 1.

The amplifier design objectives were to create a low-noise amplifier that (1) is of minimum size, (2) has the minimum thermal path to the transistor, (3) presents Γ_{opt} to the input of the transistor, and (4) minimizes the losses on the input of the amplifier. To minimize

Table 1—Optimum Noise Parameters

Freq. (GHz)	Noise Figure (dB)	Source Admittance	
		G_s (mhos)	B_s (mhos)
14.0	1.97	8.25	−3.03
14.25	2.27	2.23	−1.72
14.5	2.64	0.97	−1.46

the thermal path and the size, the transistors and substrates were designed to be mounted directly to the housing, as opposed to using a pallet and mounting the pallet to the housing. This method presents some unique fabrication problems based mainly on size, but allows the total amplifier to be housed in a chassis of dimension 1 × 0.5 × 0.5 inches.

The matching circuits were realized using microstrip matching techniques on a 10-mil alumina substrate with a chrome, copper, gold metallization scheme. The intent of the matching was to present Γ_{opt} to the input of the device and S22* to the output. Cascaded impedance transformers were used to create the desired impedance. The circuits were optimized on SuperCompact,† the microwave computer-analysis/optimization software. Bias was attained through the use of 1/4-wavelength shunt elements.

A single-stage amplifier was fabricated and assembled. Its performance is shown in Figs. 4 and 5. The matching circuits were adjusted based on the single-stage performance, and a two-stage amplifier was created. The performance of the two-stage amplifier is shown in Figs. 6 and 7. Based upon the temperature performance of the two stage amplifier, the cooling point of −50°C was chosen (see Fig. 8).

The two-stage housing is an H-type construction with the rf circuitry in the top cavity and the dc components in the bottom cavity. Waveguide-to-microstrip transitions (probe type) are used as the transmission medium for the input and output of the amplifier.

To minimize the thermal conduction into the amplifier from the external environment, an rf transmission medium with low insertion loss and high thermal resistance was required. The low insertion loss is required to avoid increasing the noise figure of the amplifier, since this component will be on the amplifier input. Waveguide components were used in this application because of their low-loss characteristics. Several different waveguide configurations were tested, and the best results (i.e., lowest insertion loss and highest thermal resistance) were achieved with a waveguide made of plastic and plated on the interior and flange surfaces.[4] The plating is designed to be thick enough to provide low-loss rf transmission, but thin enough to keep the thermal conduction to a minimum. The plastic used is an ABS polycarbonate (Cycoloy‡). Cycoloy

† Registered trademark of Comsat General Integrated Systems, Inc., Palo Alto, CA 94303.

‡ Registered trademark of Borg-Warner, Corp., Parkersburg, WV 26101.

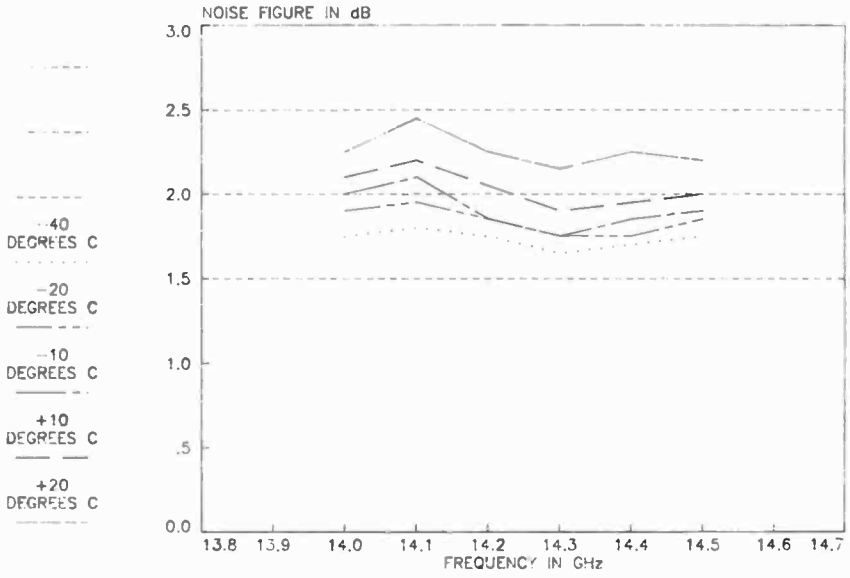

Fig. 4—Noise figure versus frequency for single-stage amplifier.

was selected because of its high thermal resistance and the well developed plating process associated with this plastic. The exterior surface of the thermal block was left unplated. A metallized tape will be applied to the exterior to provide a low emissivity surface.

The rf transmission performance of the plastic waveguide was adequate, with 0.1 dB or less of insertion loss and a return loss of greater than 25 dB. The EMI performance was adequate. During thermal testing, the plastic waveguide acted as a good insulator by maintaining a temperature difference of 65°C. By maintaining this difference, the waveguide kept the amount of heat that had to be removed from the amplifier small enough to allow the cooler to achieve an amplifier temperature of −50°C.

Thermal Design

The thermal design concentrated on three main areas of development: (1) the selection and definition of the operating environment, (2) the development and specification of components and materials, and (3) the heat-load characterization.

An active cooler (thermoelectric Peltier junction device) was selected as the cooling method. An active device was selected over a

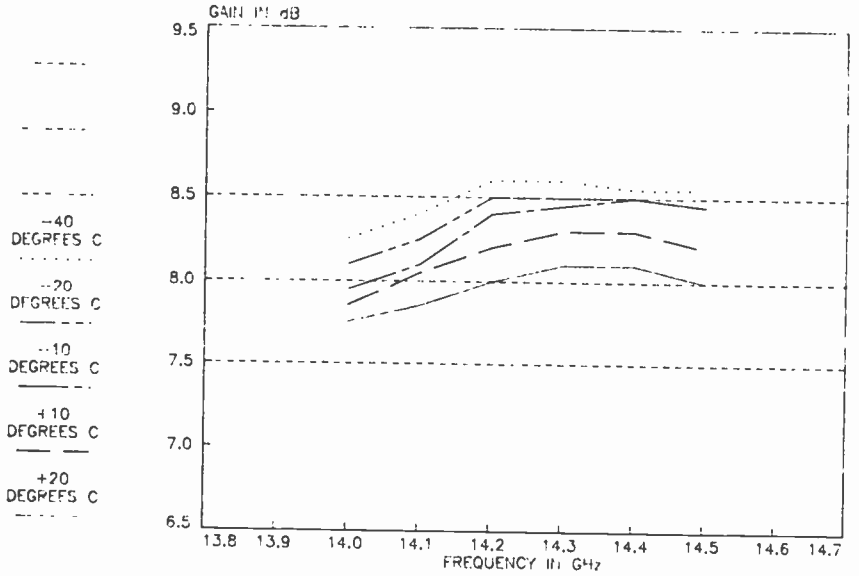

Fig. 5—Gain versus frequency for single-stage amplifier.

passive radiative type because such a device is relatively immune to spacecraft location, and the cold-side temperature can be easily regulated by controlling cooler power. The active cooler allows the CLNA to be located close to the rest of the transponder to eliminate long runs of waveguides and can be easily regulated to provide just enough cooling to maintain the temperature of the amplifier at a constant −50°C. The thermal design constraints for the CLNA are as follows:

Amplifier Temperature:	−50°C
Maximum Cooling Power:	8.0 W
Maximum Baseplate Temperature:	+15°C

CLNA must be located close to the transponder.

The maximum cooler power was determined through heat-load estimates and experiments approximating thermal environments similar to those predicted for the spacecraft. The most favorable location for the CLNA on the spacecraft to satisfy these constraints is on the north panel. In this location, the maximum baseplate temperature with the cooler operating at 8.0 W is +15°C. The maximum radiative environment is +25°C.

A thermal block diagram of the CLNA is shown in Fig. 9. A

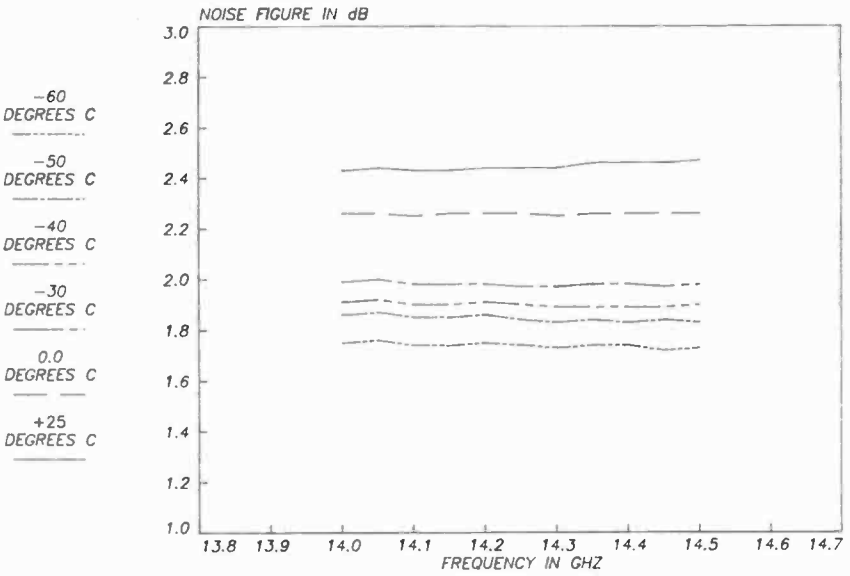

Fig. 6—Noise figure versus frequency at different temperatures for dual-stage 14-GHz amplifier.

necessary requirement of the CLNA thermal design is that all cold surfaces must have low thermal emissivity in order to reduce the amount of heat transmitted through thermal radiation. Besides the use of the thermal block, as mentioned earlier, thermal conduction was also reduced by using stainless-steel-waveguide to microstrip transitions and #32 gauge wire to bias the amplifier. Although stainless steel is heavier than the more commonly used aluminum, it has a higher thermal resistance, which makes the weight tradeoff acceptable. The #32 gauge wire has a higher thermal resistance than the usual #26 gauge.

The CLNA design must have some form of thermal stress relief between the cooler and the amplifier to provide flexibility during the cooling process when thermal contraction occurs. This stress relief is provided through the use of a strap consisting of 15 sheets of 2-mil-thick silver shaped in a "U." The bottom of the "U" is attached to the cooler, and the amplifier fits between the top ends. This strap provides the required flexibility and keeps the thermal resistance between the cooler and the amplifier to a minimum. The thermal performance of the strap has been tested, and the results indicate the flexibility is adequate and the thermal resistance, as measured by the temperature drop across the strap, is small (2°C or less).

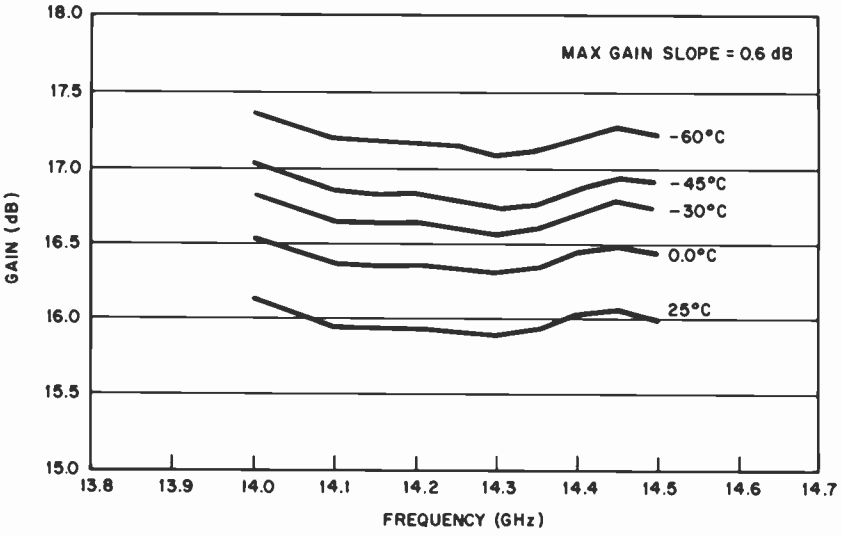

Fig. 7—Gain versus frequency at different temperatures for dual-stage 14-GHz amplifier.

An outer shield is placed around the CLNA assembly and is attached to the top and bottom plate to protect the entire structure. The shield provides EMI protection, protection from damage during testing and integration on the spacecraft, and most importantly protection from the thermal radiative environment. The shield is well coupled thermally to the bottom plate, and the temperature of this plate controls the temperature of the shield. The shield surrounds all of the cooled parts and, hence, is the thermal radiative environment for these parts. The use of this shield reduces the temperature of the radiative environment on the cooled parts by at least 10°C as opposed to having these parts see the warmer interior of the spacecraft.

The heat load of the cooler is the amount of heat the cooler must pump to achieve the desired cold temperature within the environment encountered. This heat enters the amplifier through conduction, radiation, and the dissipation of the transistors and the dc bias network. There is no convective contribution because of the vacuum environment. The most accurate method of determining the heat load is to measure the configuration to be cooled using a calibrated cooler as a calorimeter. This method was used to characterize the CLNA configuration. From the results of these tests, a cooler spec-

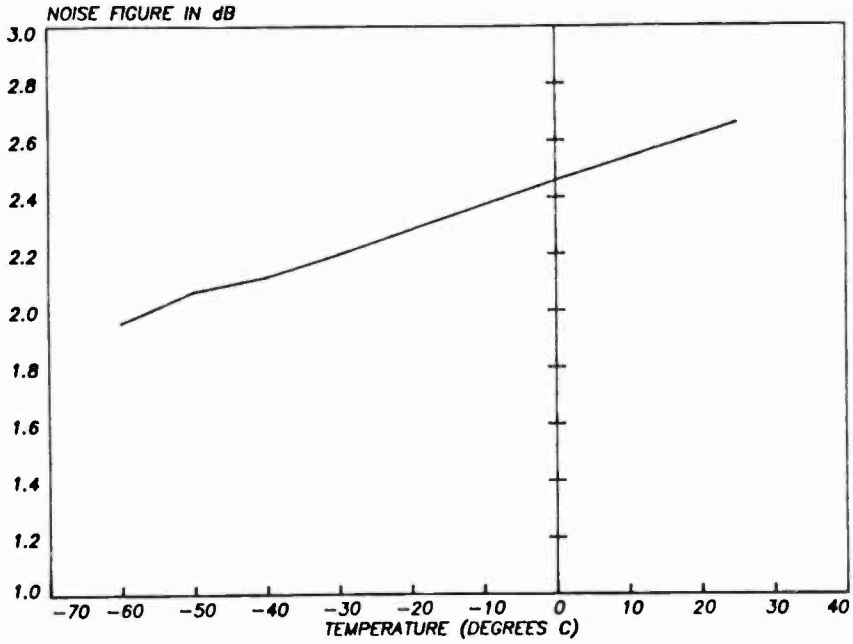

Fig. 8—Noise figure versus temperature for complete CLNA.

ification was generated and a cooler designed. The parameters of this cooler are given in Table 2.

The heat load of 790 mW shown in Table 2 is the amount of heat that must be removed from the amplifier to reduce its temperature to −50°C. Thermoelectric coolers take advantage of the heat absorption (cooling) that occurs (Peltier effect) when current passes from an n-type material (high energy level) to a p-type material (low energy level). These materials are cut into small rectangular elements whose cross-sectional area and length are designed to provide optimum cooling. The elements are arranged in the cooler so as to remove heat from one end (cold side) and transmit it to the

Table 2—Cooler Parameters

Heat Load	790 mW
Baseplate Temperature	+15° C
Cold Side Temperature	−50° C
Environment Temperature	+25° C
Maximum Input Power to Cooler	8.0 W
Cooler Current (max)	1.33 A
Cooler Voltage (max)	6.0 V

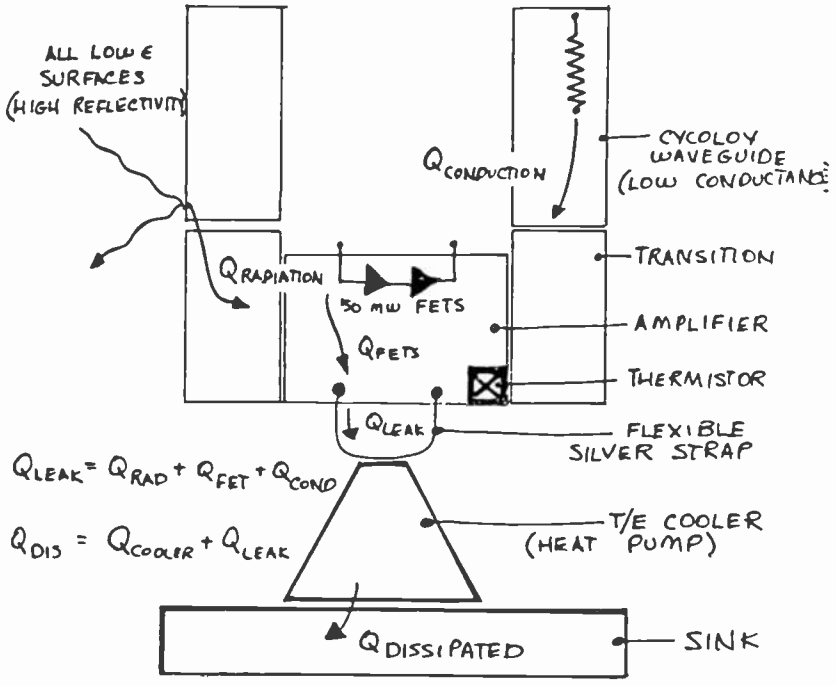

Fig. 9—Thermal block diagram.

other (hot side) and, hence, act as a heat pump. The heat load of 790 mW represents the maximum heat that must be pumped; it occurs at the hottest point in the spacecraft temperature cycle and at the end of the spacecraft life. The temperature cycle is dependent on the position of the spacecraft in relation to the sun, and the temperature change with life is caused by the degradation of the emissivity of the exterior spacecraft surfaces. The heat load will vary from 100 mW to 790 mW depending on these temperature changes. The cooler is powered by a temperature-sensing power supply (TECC; see below) that will maintain the amplifier at −50:dgC by controlling the amount of power delivered to the cooler. The actual dc operating point of the cooler will vary with the conditions of the spacecraft and will only be at a maximum for a short period of time during the spacecraft life.

CLNA DC Power

The CLNA has two power supplies. A thermoelectric cooler controller (TECC) powers the cooler, and an electronic power condi-

tioner (EPC) powers the rf FETs. Both supplies are housed in the 14/12-GHz receiver located a short distance away on the spacecraft antenna panel. These supplies derive their power from the spacecraft bus.

The TECC is a closed-loop control system that senses the rf amplifier temperature and provides the required power to the cooler to maintain the amplifier at −50°C. The control function is linear over the temperature range of −49°C to −51°C; it is fully on above this range and fully off below this range. A thermistor located in the rf amplifier provides the required temperature information to the TECC. This thermistor is also used in a temperature telemetry circuit within the TECC to provide the amplifier temperature to the ground station. The TECC is capable of providing 8.0 W at 6.0 V and 1.33 A to the cooler. The total input power required to provide the maximum power is 12.3 W. A block diagram of the TECC is shown in Fig. 10.

The EPC power supply takes power from the spacecraft bus and converts it to the power requirements of the rf amplifier. The rf amplifier requires +3.0 V with a maximum current capacity of 30 mA and −4.0 V with a maximum current capacity of 10 mA. These voltages must be free from the excess noise present on the spacecraft bus, or this noise will modulate the rf signal. The EPC performs this filtering requirement.

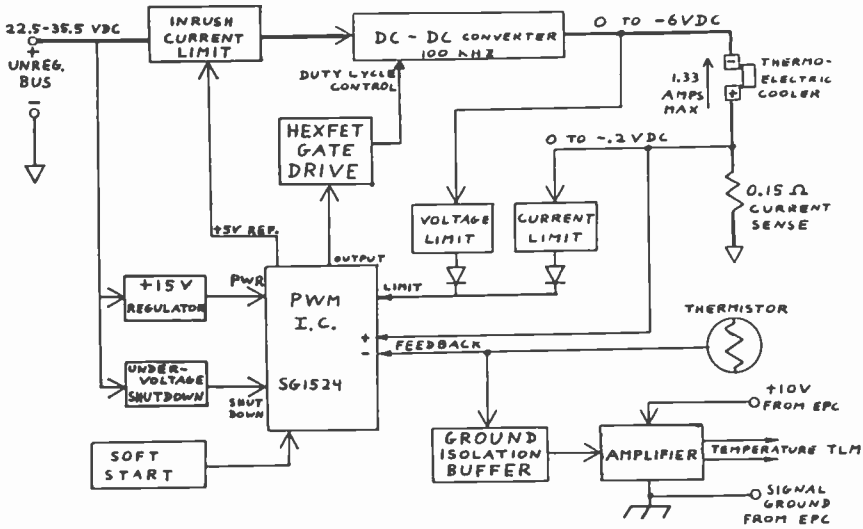

Fig. 10—Block diagram of thermoelectric cooler controller.

Mechanical Design

The main objective of the mechanical design was to package the CLNA in such a manner that it can operate in the environments specified. The final configuration is shown in Fig. 11. The total weight of the CLNA is 1.2 lbs and the outside dimensions are 4.66 × 5.25 × 4.85 inches. The amplifier assembly is shown in Fig. 12. The housing is an "H" type construction made of kovar, because the alumina substrates and transistors used in the microwave section are soldered directly to the housing and the thermal expansion coefficient of Kovar matches that of alumina. Soldering the transistors directly to the housing eliminates the thermal drop associated with the typical pallet-type construction. The microwave circuitry is housed in one cavity of the "H" frame and the dc bias components in the other. The bias is connected to the microwave section via filtercons.

The CLNA is assembled in two sections. The top-plate assembly section consists of the waveguide isolators, top plate, waveguide shims, plastic waveguides, amplifier assembly, support spacers, and amplifier bias wires (see Fig. 11). The bottom-plate assembly section consists of the bottom plate and the thermoelectric cooler. The waveguide shims in the top assembly are used to adjust any tolerance build-up problems that occur in assembly. Side plates are attached to the support spacers to provide stiffening for vibration loading. A thin aluminum cover is attached around the entire unit and serves as an EMI and thermal shield. A photograph of the engineering model with the side plates and thermal shield removed is shown in Fig. 13.

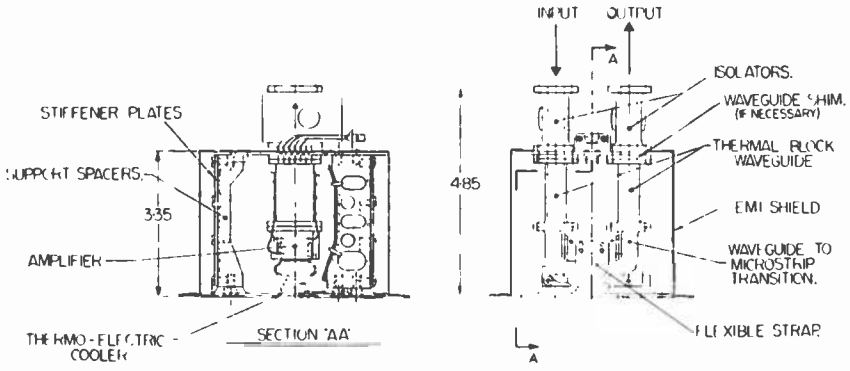

Fig. 11—Front and side sections of CLNA (see Fig. 13).

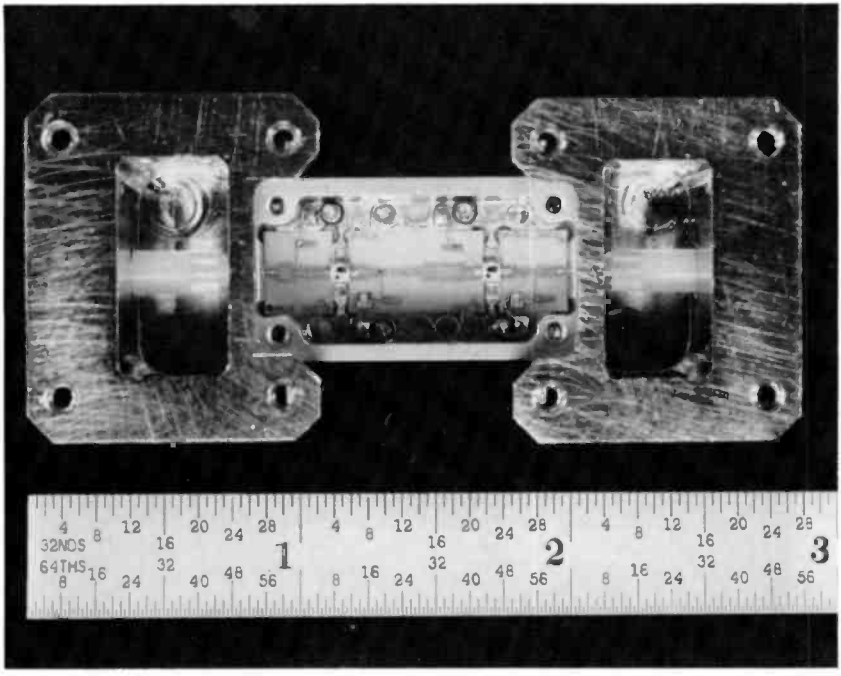

Fig. 12—Amplifier assembly.

This configuration is designed to withstand the vibration environment that will be encountered during spacecraft launch.

Performance of Engineering Model

An engineering model was assembled and tested in a thermal vacuum chamber. The thermal vacuum test setup, shown in Fig. 14, was designed to represent the actual spacecraft environment. On the spacecraft, the CLNA will be mounted to a heat spreader of a size that will keep its baseplate at $+15°C$ with full cooler power. The temperature of this spreader is determined by the spacecraft external environment and the cooler power. To simulate these conditions in the test, the CLNA was mounted to a radiator plate that was tightly coupled to a heat exchanger (see Fig. 14). The radiator plate and heat exchanger simulated the spacecraft heat spreader and the external environment, respectively. The internal spacecraft environment was simulated by a temperature-controlled shroud placed inside the thermal vacuum chamber around the test setup.

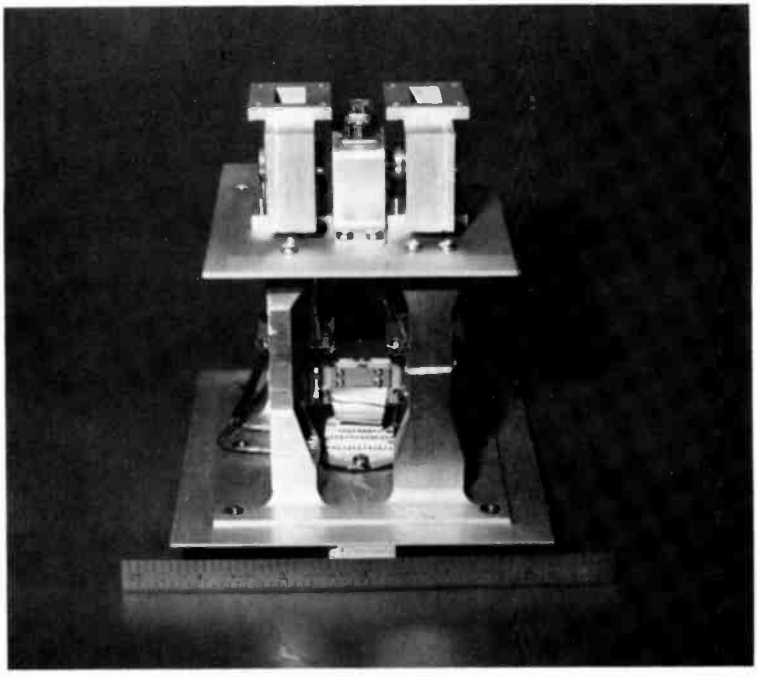

Fig. 13—Engineering model of CLNA with shield and stiffener plates removed.

The thermal performance and cooler power required is given in Table 3. The noise figure and gain performance is shown in Figs. 15 and 16, respectively. The cooler was powered by a controller

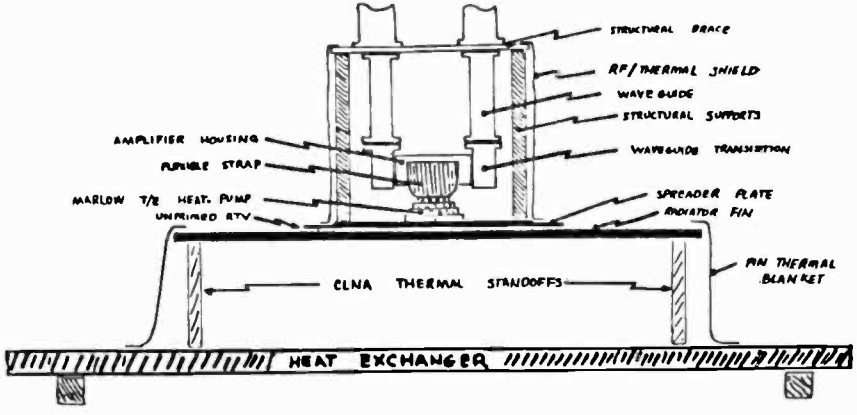

Fig. 14—Thermal vacuum test setup.

Table 3—Thermal Performance and Cooler Power

Temperature (°C)				Heat Load (mW)	Cooler Power (W)
Environment	Heat Exchanger	Base-plate	Amplifier		
+25	−28	−8	−50	250	2.0
+25	−10	+15	−50	480	5.0
0	−28	−18	−50	200	0.5
0	−56	−36	−50	40	0.2

which was capable of maintaining the temperature at −50°C (close loop operation) or delivering maximum power (8.0 W).

In the worst-case predicted environment (−28°C heat exchanger and +25°C shroud temperature), the power required to maintain the amplifier at −50°C was only 2.0 W; the maximum allowable is 8.0 W. This situation occurred because the baseplate of the CLNA stabilized at −8°C instead of the predicted +15°C. The +15°C was calculated with the assumption that the cooler would draw 8.0 W. When the temperature of the baseplate was allowed to rise to +15°C, the cooler required 5.0 W of power to achieve −50°C. The

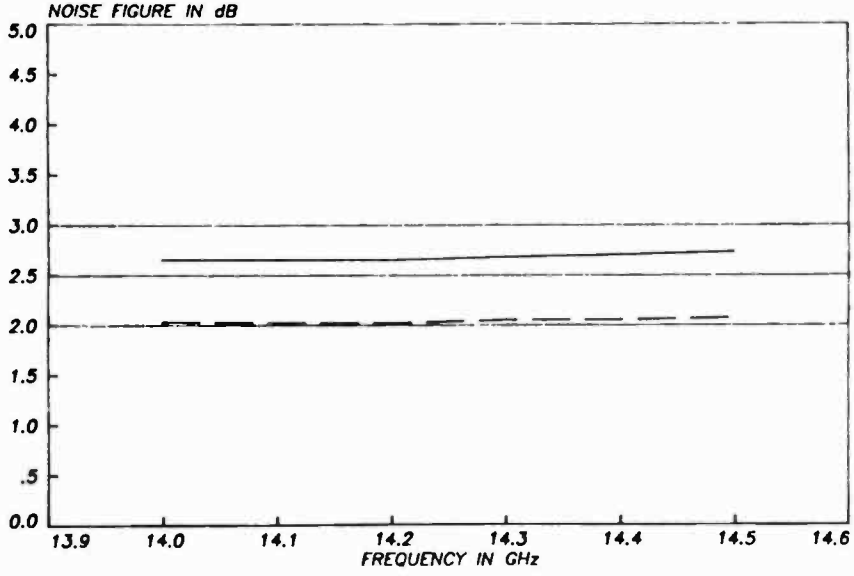

Fig. 15—CLNA noise figure versus frequency at amplifier temperatures of +25°C (solid curve) and −50°C (dashed curve). Test performed in vacuum of 10^{-5} Torr.

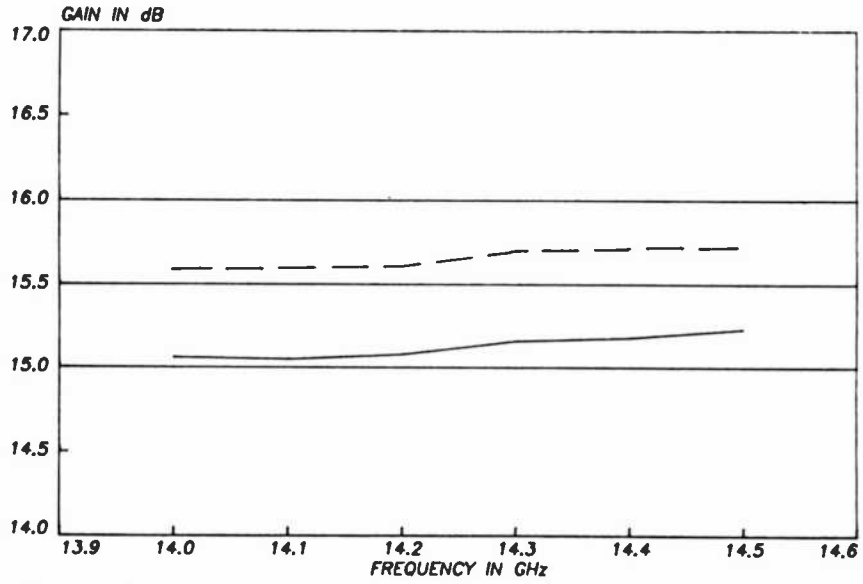

Fig. 16—CLNA gain versus frequency at amplifier temperatures of +25°C (solid curve) and −50°C (dashed curve). Test performed in vacuum of 10^{-5} Torr.

rf performance specification was achieved with a maximum noise figure of 2.1 dB and a minimum gain of 15.0 dB.

Conclusion

A cooled low-noise amplifier has been successfully developed with a noise figure of less than 2.1 dB and a minimum gain of 15.0 dB. When the CLNA was operated at the worst-case conditions of temperature, the power required to maintain −50°C was within the maximum specification of 8.0 W. Since these worst-case conditions will only occur at the end of life and then periodically throughout the seasonal variation of the spacecraft, the CLNA will actually be operating at significantly less power consumption. The first space application of the CLNA will be on the Satcom Ku-band communication satellite due for launch in 1985.

Acknowledgments

The authors wish to acknowledge the technical assistance provided by R. Wondowski, E. Mykietyn and G. Pallas in the areas of fabrication and assembly and M. McIntyre and D. Kemp in the areas of

electrical and rf testing. The guidance and insight of H. Zelen, R. McCann, E. Morse, P. Wise and H. Strickberger provided invaluable in the completion of this task and deserve special thanks.

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20-GHz Lumped-Element GaAs FET Driver Amplifier

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Abstract—A wideband lumped-element 20-GHz driver amplifier using GaAs FET chip devices for a 30/20-GHz communications satellite is described. Also described is a wideband 17- to 22-GHz low-loss waveguide-to-microstrip transition developed to provide the input and output connections to the microstrip amplifiers. An rf output power level of 17 dBm and 12-dB gain over the 17.7- to 20.2-GHz band was achieved using two stages.

1. Introduction

Increasing use is being made of the 30/20-GHz frequency range for satellite communications. Downlink, 20-GHz travelling-wave-tube amplifiers (TWTAs) require linear driver amplifiers for added gain capability. The 20-GHz driver amplifier described here uses lumped-element matched GaAs FET chip devices and provides an output level greater than 13 dBm to drive the TWTAs.

At 20 GHz, a waveguide is the most common transmission medium due to its low loss characteristics. The most convenient media for impedance matching GaAs FET amplifiers, however, are 50-ohm microstrip input and output sections. Therefore, a waveguide-to-microstrip transition was developed. Lumped-element matching networks (bond wires, ribbons and capacitors) are used, since they incorporate the parasitic elements in the device-to-circuit interface, thus allowing maximum attainable power and gain by the device.[1] Smaller circuit sizes (less weight) and wider bandwidths are also possible with lumped-element matching.[2]

Single-stage lumped-element matched amplifiers mounted on gold plated copper carriers were developed individually. The input

amplifier, which uses an AT-8041 FET,† was cascaded with the output amplifier, which uses a DLX-3504A FET.*

The waveguide-to-microstrip transition is discussed first. The individual stages of the amplifier are then discussed, together with the chip carrier design. Finally test results for the full amplifier are presented.

2. Waveguide-to-Microstrip Transition

The 20-GHz transition was designed for a WR-42 rectangular waveguide and a microstrip using a 15-mil quartz substrate.[3,10] The design of such a transition is essentially that of an impedance transformer. There are, however, four different definitions of impedance for rectangular waveguides: voltage-current, power-voltage, power-current, and E-H. For the impedance-matching applications, studies by Chen[4] and Mihran[5] have shown that for ridge waveguides the V-I definition is the most convenient. A four-step Chebyshev quarterwave transformer method was used to transform the waveguide impedance to the 50 ohms of the microstrip. The ridge width is kept constant and the gap is varied to obtain the desired impedances of the transformer. Corrections in the length of the quarterwave transformers were calculated using rectangular waveguide approximations. The ridge waveguide was considered to be equivalent to a rectangular waveguide, with the guide wavelength given by the ridge-waveguide parameters.

Higher order modes are generated at the wageguide-microstrip junction. To prevent these higher order modes from being transmitted, resulting in losses, a small rectangular cover with cutoff waveguide dimensions is placed at this junction (Fig. 1). The dimensions of this cover were calculated using the approximate formula, given by Schneider,[8]

$$f_c = \left[\frac{C}{2a}\right]\left[1 - \frac{h\,(E_r - 1)}{b\,E_r}\right],$$

where f_c is the first higher-order-mode cutoff frequency, a the cover width, b the cover height, h the substrate thickness, and E_r is the relative dielectric constant. According to this equation, when a = 0.24 inch and b = 0.17 inch, then f_c = 23.8 GHz, which is above the upper band edge (20.2 GHz). Fig. 1 shows the two waveguide-

† Avantek Inc., Santa Clara, CA 95051.
* Dexcel Div., Gould Inc., Santa Clara, CA 95050.

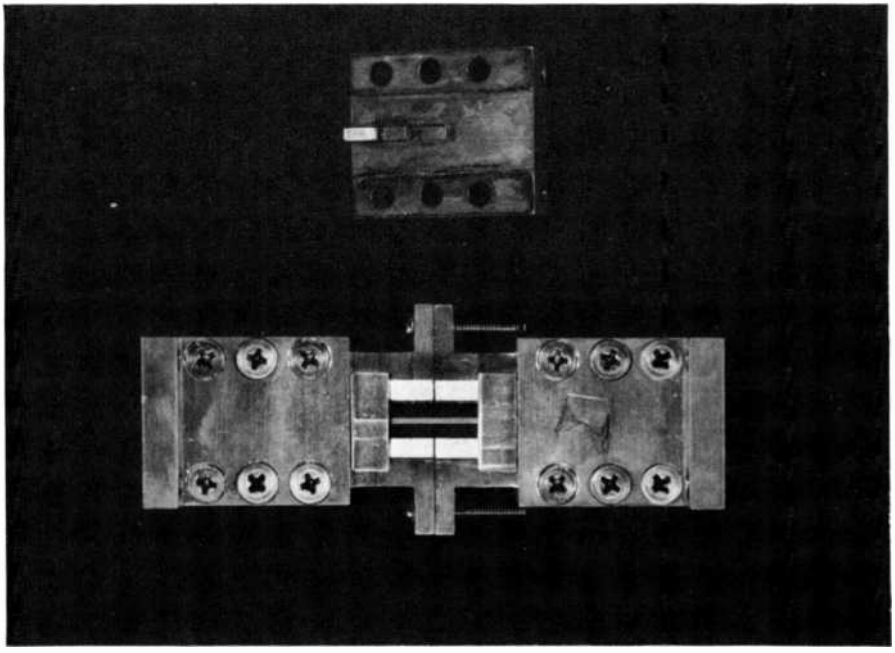

Fig. 1—Waveguide-to-microstrip transition (back to back).

to-microstrip transitions connected back-to-back for testing purposes. To test the amplifier, it would be placed in the middle between the two transitions.

The two transitions, including an 0.88-inch-long microstrip line inbetween, were first tested with a scalar network analyzer for insertion loss and return loss. The measured insertion loss was 0.5 dB and was flat for both transitions together (0.25 dB/transition) from 17 to 22 GHz; return loss was about 20 dB.[10]

The full S parameters were measured for single transition on an automatic network analyzer, using through-short-delay (TSD) calibration and deimbedding procedures.*[11] The results are shown in Table 1.

3. Chip Carriers and Matching Network

Avantek AT-8041 and Dexcel DLX-3504A GaAs FET chip devices were used in the amplifier chain. These devices were chosen for their low noise figure and because they provided the required power

* This program, called PLANA, is available under license from RCA Software Marketing, RCA Laboratories, Princeton, NJ 08540.

Table 1—*S* Parameters for Waveguide-to-Microstrip Transition

Freq. (GHz)	*S*11		*S*21		*S*12		*S*22	
17.0	−18.2	−175.8	−.15	−66.4	−.15	−66.4	−18.9	−134.0
17.5	−16.9	161.1	−.20	76.2	−.20	76.2	−17.0	168.1
18.0	−17.6	149.4	−.25	39.9	−.25	39.9	−17.7	105.8
18.5	−20.4	141.6	−.18	4.2	−.18	4.2	−20.6	48.8
19.0	−26.2	139.4	−.22	−31.9	−.22	−31.9	−26.9	−21.5
19.5	−39.0	−55.0	−.23	−66.5	−.23	−66.5	−36.6	167.5
20.0	−28.0	−38.9	−.22	79.7	−.22	79.7	−29.1	8.07

output. Two designs using the AT-8041 were developed. One used resistive matching on the output to make the amplifier highly stable ($K \gg 1$); the other provided higher gain using reactive matching, while still maintaining the stability factor $K > 1$.

The chip carriers were made of copper for good thermal conductivity. The carriers were then gold plated for bonding purposes. The FET chip and the lumped-element matching network were all assembled on the same carrier, as shown in Fig. 2. The dimensions of the carrier are such that the top bonding surfaces of the GAAs FET chip and other matching network components are all at the same level after mounting. This is done for ease of bonding and to lend itself easily to automatic bonding.

Fig. 3 shows a chip carrier. The chip is mounted on a separate narrow chip carrier, which is then mounted onto the amplifier fixture. This arrangement enables the chip to be mounted with any temperature solder/epoxy, independent of the rest of the circuit.

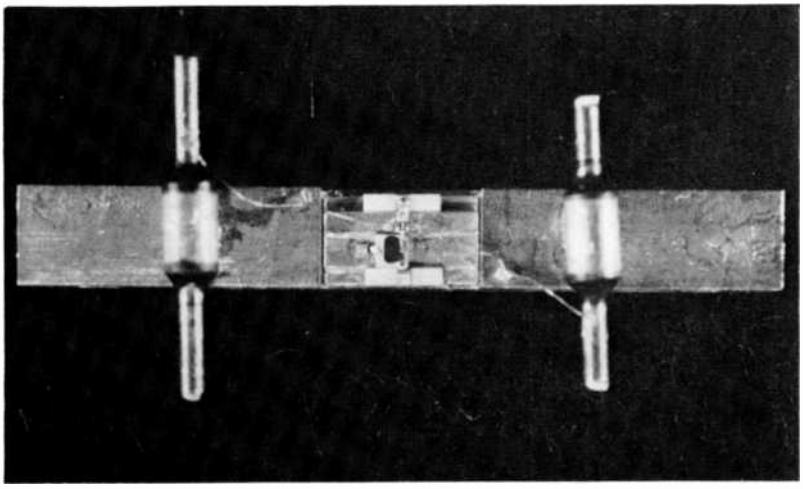

Fig. 2—Resistively matched AT-8041 amplifier assembly.

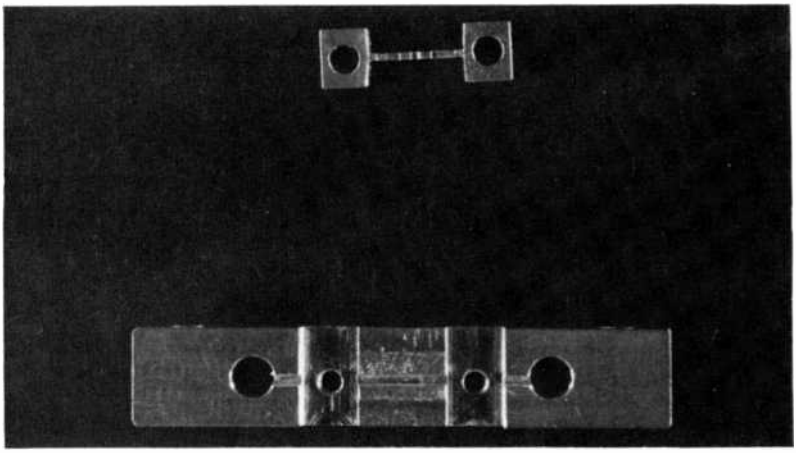

Fig. 3—Chip carrier (above) mounted on amplifier fixture (below).

Also, the chip can be replaced easily without affecting other parts of the amplifier.

Very small sections of 50-ohm microstrip line are added at the input and output of the amplifier (Fig. 2). This enables connection between the matched amplifier and the waveguide-to-microstrip transitions. These short microstrip sections also allow capacitive stub tuning to be employed, if necessary, reducing the need to tune fragile 0.7-mil bond wires.

A 25-mil-thick alumina substrate is used for the microstrip. Since the microstrip sections are short, using alumina instead of quartz does not introduce moding problems.

The amplifier was tuned by three methods: (1) changing the height of the bond wires above ground; (2) spreading wires (when parallel wires are used); and (3) capacitive stub tuning at the input or output microstrips. Very little or almost no tuning was done using bond wires, however, due to the difficulty of this operation. Tuning was primarily accomplished by minimal tuning on the short microstrip lines.

4. AT-8041 Chip Amplifier Design

Avantek low-power, low noise-figure AT-8041 devices were used in developing two input amplifier stages for the driver. In designing these amplifiers, the matching network was optimized mainly for gain and flatness.

To enhance the amplifier's stability ($K >> 1$), a resistive matching network is used (see Fig. 4). The circuit was optimized for a gain of

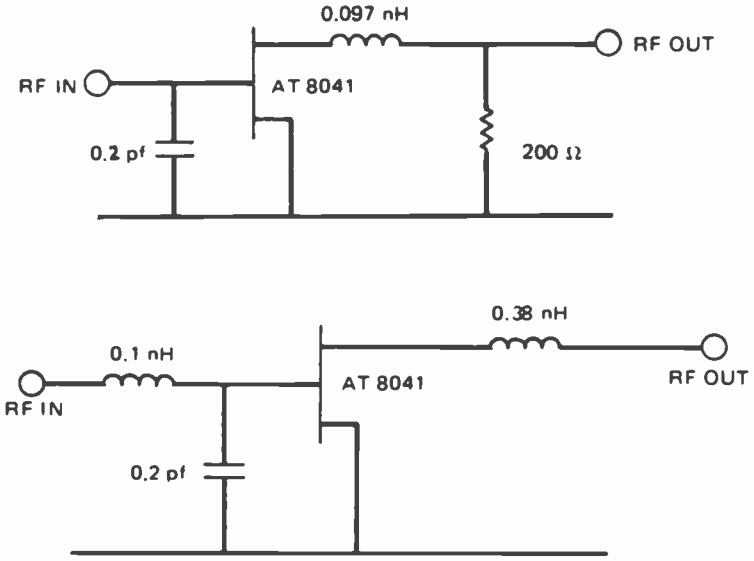

Fig. 4—Resistive (top) and reactive (bottom) matching networks for AT-8041 amplifier stage designs.

5 dB. Table 2 shows the SuperCompact* calculated response of this amplifier.

A chip resistor and an ultrahigh-Q chip capacitor were used for the network's R-C components. The inductance was obtained using 0.7-mil-diameter gold bonding wire. The length of the wire was calculated from standard equations.[9] For the connection between the coupling capacitor and the input microstrip and between the

* Registered trademark of Comsat General Integrated Systems, Inc., Palo Alto, CA 94303.

Table 2—Computer Generated Response of AT-8041 Chip (Resistive Matching)

Frequency (GHz)	$S11$ (dB)	$S22$ (dB)	$S21$ (dB)
17.2	−5.43	−7.89	4.91
17.6	−5.99	−8.00	5.04
18.0	−6.69	−8.16	5.13
18.4	−7.54	−8.29	5.10
18.8	−8.66	−8.54	5.06
19.2	−10.23	−9.00	5.06
19.6	−12.47	−9.68	5.04
20.0	−15.70	−10.49	4.96
20.4	−17.72	−11.15	4.96
20.8	−17.00	−11.80	4.96

Table 3—Computer Generated Response of AT-8041 Chip (Reactive Matching)

Frequency (GHz)	S11 (dB)	S22 (dB)	S21 (dB)
17.2	−5.60	−6.54	7.33
17.6	−6.20	−7.15	7.43
18.0	−6.96	−7.85	7.48
18.4	−7.87	−8.83	7.40
18.8	−9.04	−10.03	7.27
19.2	−10.43	−12.08	7.14
19.6	−11.97	−15.39	6.93
20.0	−13.43	−20.63	6.64
20.4	−13.51	−26.38	6.47
20.8	−12.77	−22.62	6.30

resistor and the output microstrip, short 10-ml-wide ribbons were used to minimize the series parasitic inductance (Fig. 2).

A second single-stage amplifier, requiring 6-dB gain, was developed using the AT-8041 chip. It employs a reactive lumped-element matching network (see Fig. 4). Table 3 shows the computer simulated response of this amplifier. Bond wires and chip capacitors were used to realize the element of the reactive network. The assembly configuration is basically the same as that for the resistive network.

5. DLX 3504A Chip Amplifier

A Dexcel DLX 3504A device was used in the last stage of the driver amplifier. The amplifier is matched using an *L-C-L* network (T network) for both input and output. The matching network was first designed on a Smith chart and then optimized, using Super-Compact, for a gain of 5.2 dB across the frequency band and for minimum *S*11 and *S*22 parameters.

For both the input and output microstrip sections, 15-mil quartz substrates are used. The width of the substrate was 200 mils in order to prevent any higher order modes from being transmitted.[8]

6. Performance

5.1 Individual Amplifiers

Fig. 5 shows the measured gain of the resistively matched AT-8041 chip amplifier. The FET was biased at V_{ds} = 2 V and I_{ds} = 16 mA. This bias level provided enough gain while minimizing power consumption.

Fig. 5 also shows the measured gain response for the reactively matched AT-8041 chip amplifier. The bias level for this amplifier

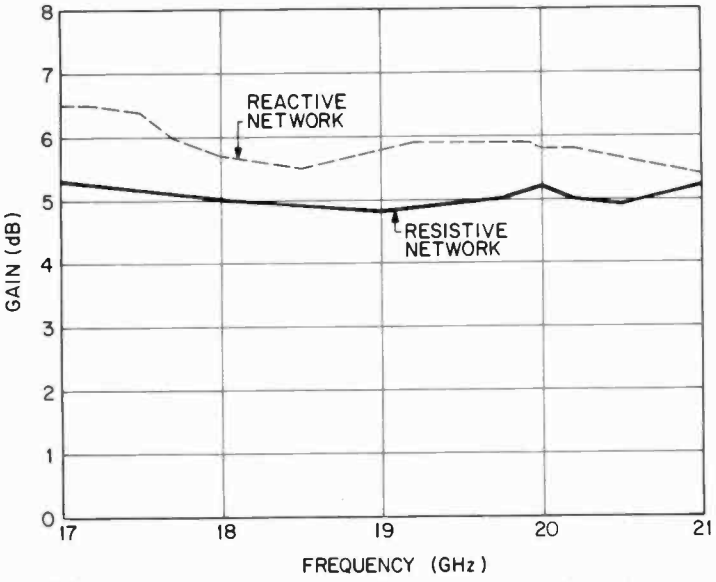

Fig. 5—Measured gain responses of resistively and reactively matched AT-8041 amplifiers.

was V_{ds} = 3 V and I_{ds} = 25 mA. The actual gain is slightly lower than the design value but is reasonably flat across the band.

The Dexcel's DLX-3504A amplifier was also tested using the waveguide-to-microstrip transitions. Since two parallel bonding wires were used for this amplifier, it was possible to tune by changing the separation between the wires. A 50-ohm resistor in series with the gate bias choke was used to suppress low-frequency oscillations.

Figs. 6a and b show the measured amplifier responses. As shown by the power-in versus power-out relation, the amplifier does not reach 1-dB compression, even at the +17-dBm level.

5.2 Cascaded Amplifiers

After each amplifier was tested and optimized individually for maximum gain and flatness, the amplifiers were cascaded with one output amplifier. At first, the reactively matched AT-8041 chip amplifier stage and DLX-3504A chip amplifier stage were cascaded without the use of isolators. After slight capacitive tuning of the microstrip sections, the responses shown in Figs. 7a, b, and c were obtained. The measured performance with the two stages cascaded are shown in Table 4.

Table 4—Measured Performance of Cascaded Amplifiers

Frequency	17.7 GHz to 20.2 GHz
Output Power	+17 dBm at 1 dB compression point
Gain	12 dB
Gain Flatness	±0.5 dB
VSWR	2.3:1
Efficiency	12.4%

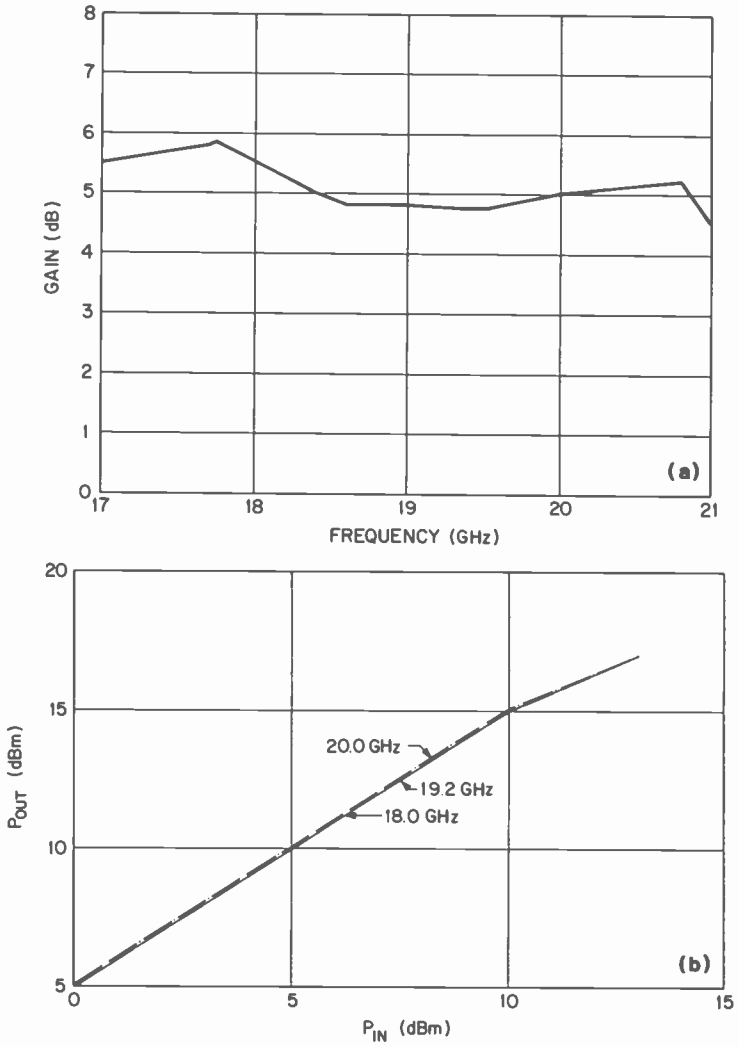

Fig. 6—(a) Gain response of DLX-3504A amplifier and (b) power in versus power out for the same amplifier.

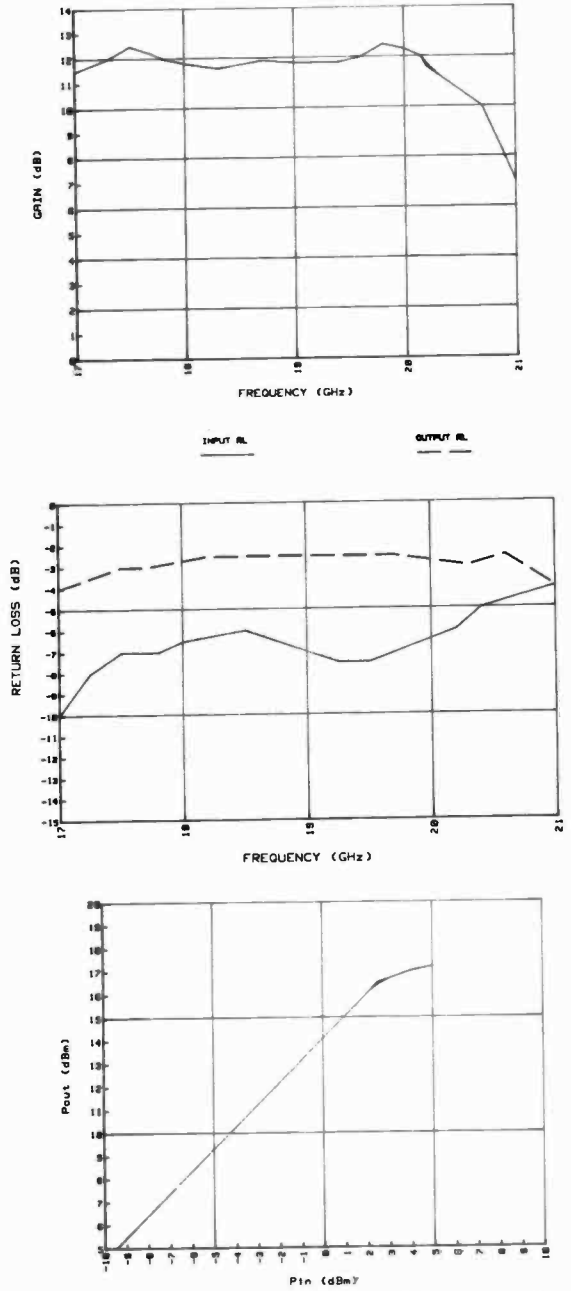

Fig. 7—(a) Gain response, (b) return loss, and (c) power in versus power out for the cascaded amplifier.

7. Conclusion

The use of lumped-element matching networks and short microstrip lines for tuning has been demonstrated for a 20-GHz driver amplifier. This facilitated ease of tuning (and of manufacturability) by not requiring adjustment of fragile bond wires. The small circuits led to small size and low weight, a premium in space applications. Using this approach, a driver amplifier with an output power of +17 dBm at 1-dB compression has been developed.

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Limiting Amplifier for Instantaneous Frequency Measuring System*

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Abstract—The microwave integrated-circuit limiting amplifier (LA) described in this article was designed to provide a constant output signal level over a wide (8 to 11 GHz) frequency band while the input signal level varies over the range of −50 to 0 dBm. A salient feature of the LA is the slope of the output power versus frequency response. This slope allows the LA to function as a wide-band limiter/discriminator when a suitable detector is added to the output.

Introduction

Frequency memories are used in electronic warfare systems to instantaneously capture and store the frequency of a received signal, be it from an enemy search radar or the guidance radar of an incoming missile. The objective is to direct a deceptive signal, at the proper frequency, to the radar receiver and give it erroneous range information on the actual position of the target. In the case of a radar-homing missile, the transmitted signal (i.e., the deceptive signal) is varied in time to cause the guidance system to steer the missile so that it misses the target and continues harmlessly on its way to self-destruction.

The frequency of the signal received by the deceptive jammer, obviously, must be determined with great speed and accuracy. The accurate determination of the incident frequency depends on a frequency discriminator that requires a constant signal level to operate properly. However, the signals arriving at the receiver can

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come from a wide variety of sources that transmit signals with widely varying amplitudes and from different, and sometimes fast moving, locations. This variety of signal levels makes it necessary to normalize the received signal before frequency discrimination. The limiting amplifier (LA) described in this paper was designed to provide the required constant signal level to the discriminator over a wide frequency band while the received signal level is in the range of −50 to 0 dBm (a 100,000:1 signal-level variation).

Design

The limiting-amplifier objective specifications are as follows:

Frequency Range: → 8 to 11 GHz
Input Signal Level: → −50 to 0 dBm
Output Power Level: → > +3 dBm

Since the required minimum output power is +3 dBm and the minimum input signal is −50 dBm, a minimum overall saturated gain of 53 dB is required. The design proceeded on the assumption that the required gain was 60 dB to allow for a margin of safety.

Fig. 1 shows the block diagram and gain budget for the proposed amplifier. The gain budget indicates that nine stages were needed to meet the requirements of this program. The output power was estimated to be 9.1 dB.

Conservatively assuming 7-dB gain per stage for the low-noise stages, 7.5 dB for the high-gain stages, and 5 dB per stage for the limiting stages and allowing for a total loss of 2.4 dB in four interstage isolators, we required two 7-dB stages, five 7.5-dB stages, and two 5-dB stages. This configuration will give a theoretical gain of 59.1 dB.

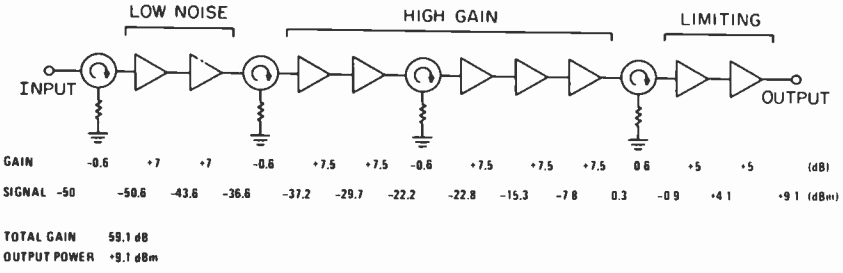

Fig. 1—Limiting amplifier block diagram and gain budget.

Table 1—Manufacturer's Transistor Data

Transistor	P_o (dBm) @ 1 dB comp. 12 GHz	Noise Figure (dB) 8 GHz	Noise Figure (dB) 12 GHz	Assoc. Gain (dB) 8 GHz	Assoc. Gain (dB) 12 GHz	Noise Measure (dB) 8 GHz	Noise Measure (dB) 12 GHz	Cost each ($) 1–9	Cost each ($) 10–49
NE13783	6	1.2	1.9	11	9	1.29	2.12	64	63
NE46383		2.2	3.9	13	10	2.29	4.18		60
NE46385		3	4.1	12	9	3.14	4.47	71	68
NE67383	14.5	1.0	1.5	11.5	10	1.07	1.64	115	105

The transistor selection process started with a review of manufacturers' data sheets to compare typical data. As an empirically derived rule of thumb, a safety factor of approximately 20% was imposed on the manufacturer's single-frequency information to allow for the degradation caused by the matching network losses and the wide-band performance requirement. Table 1 is a compilation of the technical data on the transistors that were considered for this application and includes cost information.

The NE 46383 was the first transistor to be evaluated for this application, since it was thought that a dual-gate device would offer some advantages due to its switching and gain control characteristics. However, any attempts at making measurements on this packaged device showed it to be unstable in the frequency range of interest.

Using CAD, it was found possible theoretically to increase stability by adding a resistor in the output circuit, but this reduced the gain to an unusable level. At this point it was decided to use the NE 13783 for the amplifier design, since it was more stable and we had had considerable design experience with it on other programs. It cost slightly more than the NE 46383, but that was far outweighed by the potential instability problem of the NE 46383.

Preliminary evaluation of the selected transistor included the usual network analyzer measurements using the Thru-Short-Delay (TSD) techniques, plotting gain circles, and (with these results) designing the matching networks.* We found that the gain of these stages was sufficiently high for an eight-stage chain to be theoretically adequate. Several chains were assembled before any of them

* These procedures were discussed in the author's paper in the Dec. 1983 *RCA Review*, pp. 537–550.

were evaluated in the final system. It was there that we found that more gain would be required to provide an adequate margin at the −50-dBm input power level. The additional gain took the form of an add-on housing containing a two-stage circuit carrier. This small unit was placed between the two larger housings.

Results

The overall response of the three-housing chain is shown in Fig. 2(a). As can be seen, with 3 volts on the drains of all of the transistors, the amplifier was not limiting well at an input-signal level of −50 dBm. Reducing the drain voltage to 2 volts on all four transistor stages in the output housing produced the results shown in Fig. 2(b), where the amplifier was limited at the −50 dBm level. This change in voltage also reduced the output-signal variation to 0.6 dB peak-to-peak as opposed to a 0.9-dB peak-to-peak variation at 3 volts.

The response shown in Fig. 2(b), while smoother than that of Fig. 2(a), is not adequate for the system due to the remaining amplitude ripples, since the discriminator is very sensitive to small variations in signal amplitude. If there are two input signals very close together, these variations could result in the same discriminator output voltage at two different input frequencies. The system then could not determine which frequency was actually being received.

The discriminator output voltage had a negative slope, i.e., decreasing output with increasing frequency. The steeper the slope of the overall system frequency response (within limits), the better the differentiation between closely spaced frequencies. It was determined that the system performance would be enhanced if the LA had an output power level versus frequency response that sloped in the same manner as the discriminator's.

The judicious placement of a long stub in the last amplifier stage produced the desired negative slope response from the LA chain. Various stub lengths were tried until an optimum configuration was found. If the stub length is too long, the amplifier output at the high-frequency end of the band is too low in power. If too short, the positive sloping portions of the response are not eliminated. Fig. 3 shows the LA's response to several different stub lengths.

The response of the final LA chain is shown in Fig. 4. The minimum gain was 59 dB at the high end of the band and at least 63 dB at the low end. Over some portions of the band, the chain is limiting with input signals as low as −60 dBm.

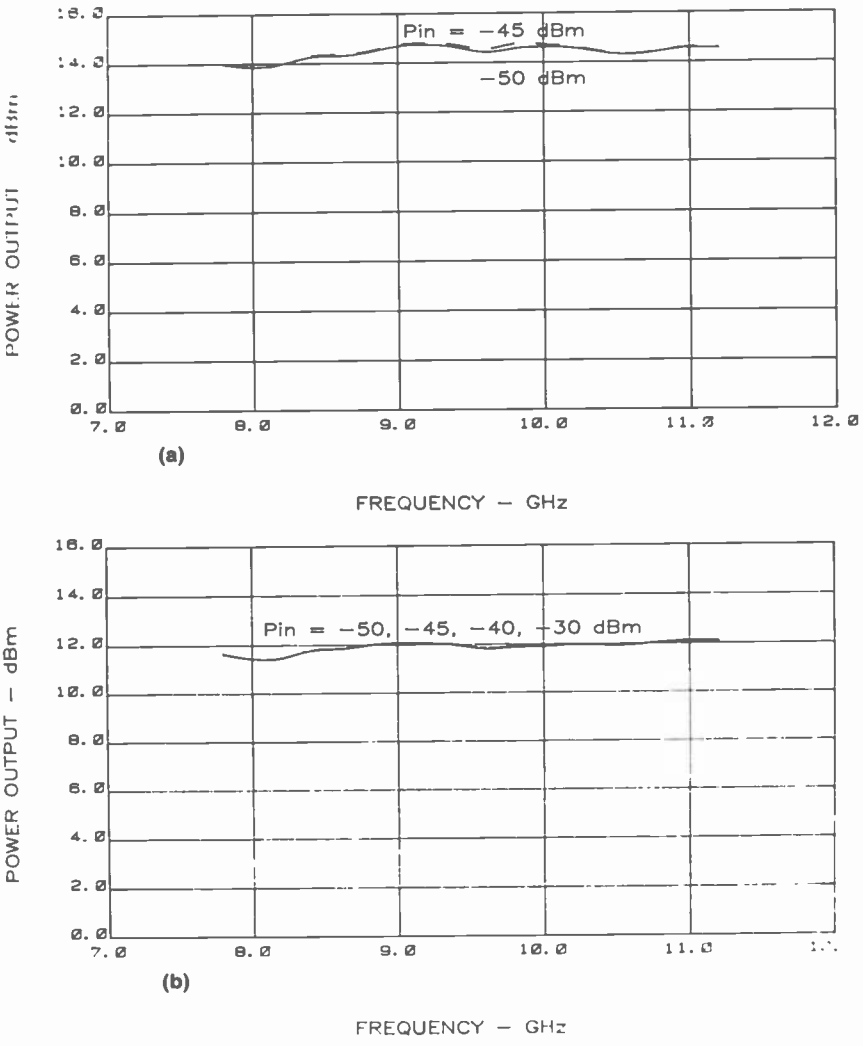

Fig. 2—Overall response of limiting amplifier (three-housing chain) (a) with three volts on all transistor drains and (b) with two volts on all drains.

Assembly

The final LA chain was assembled into three gold-plated brass housings. The amplifier stages were assembled in pairs with two amplifier stages per circuit carrier. As can be seen in the block diagram of Fig. 5, with the exception of the add-on housing, each pair of

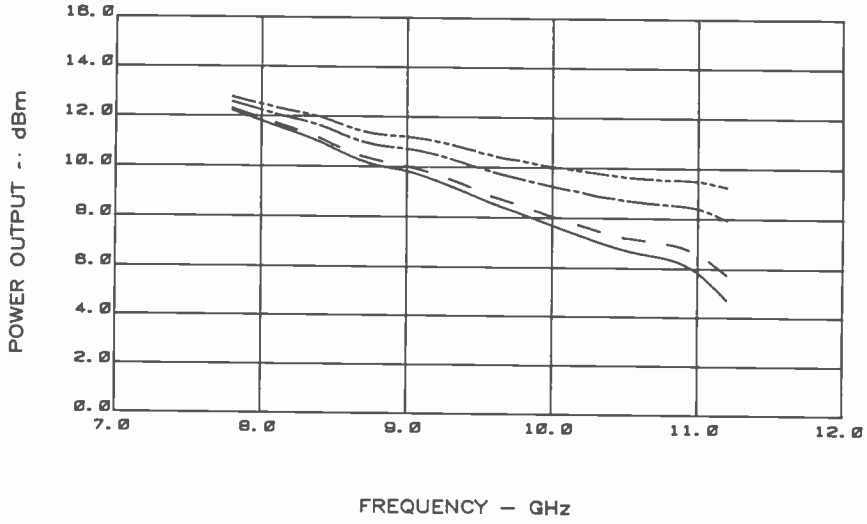

Fig. 3—Limiting amplifier response to different stub lengths. The top curve represents the shortest stub and the bottom curve the longest stub.

stages was preceded by a drop-in isolator. Two of these assemblies (isolator and circuit carrier) were placed in a housing forming a four-stage unit. The two stages in the center of the amplifier chain consist of one two-stage carrier in a separate housing.

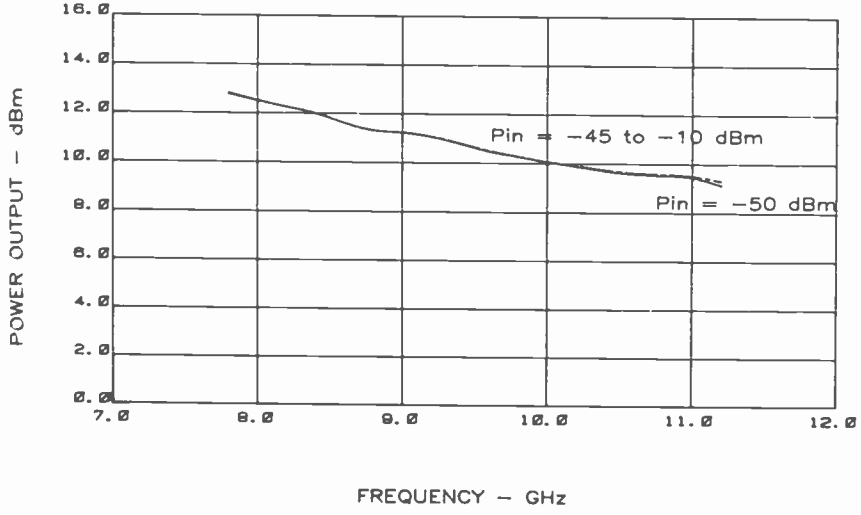

Fig. 4—Final response of limiting amplifier.

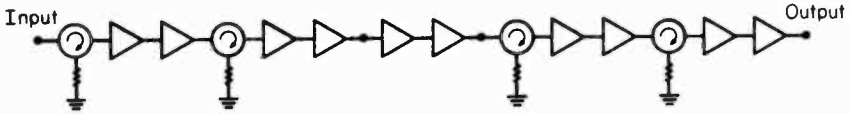

Fig. 5—Block diagram of final design of limiting amplifier. The frequency range is 8 to 11 GHz; the input power range is from −50 to 0 dBm; and the output power > +9 dBm.

To stabilize the amplifier, the lid on each of the housings was covered with microwave absorbent material. Fig. 6 is a photograph of the amplifier chain with the lids removed.

Several improvements in the design of this amplifier chain are possible. Limiting diodes could be added at several places in the chain to reduce the hard over-drive. The addition of bandpass filters at various points in the chain would probably reduce the ripples by eliminating harmonics that cause unpredictable results. Last, the series gate resistors could be adjusted to optimize amplifier performance.

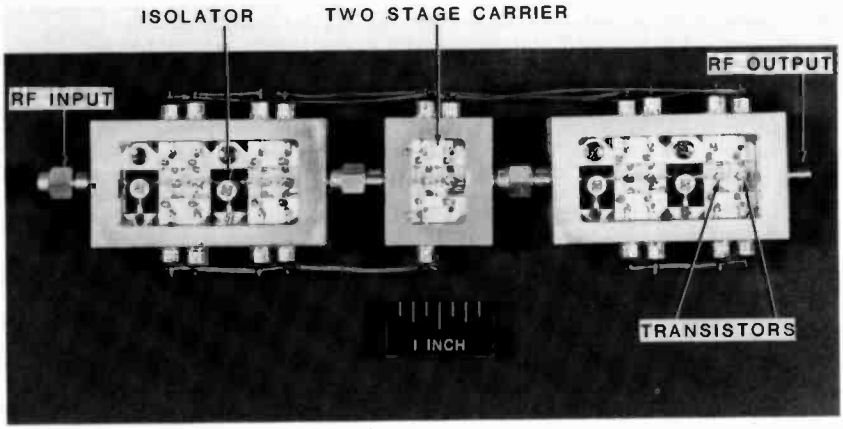

Fig. 6—Limiting amplifier chain with lids removed.

Acknowledgments

The author wishes to acknowledge the contributions of S. P. Grober for his excellent assembly skills and assistance in testing these amplifiers, D. D. Mawhinney for defining system requirements and his suggestions for amplifier improvement, and H. J. Wolkstein for his guidance and encouragement.

Patents Issued to RCA Inventors—Third Quarter 1984

July

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August

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September

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He joined RCA's Microwave Tube Operation in 1961. After an assignment in the Pencil Tube Design and Applications group, he worked on microwave solid-state design projects as part of the Advanced Development activity; there he developed solid-state oscillators for radiosonde applications and projectile telemetry transmitters. In 1972, he transferred to the RCA Solid State Division, supervising the fabrication and testing of microwave power amplifiers for military and space applications. He also served as type engineer for thick-film hybrid devices used in heart pacers. After a stay at Microwave Semiconductor Corp. in 1977–78, Mr. Askew returned to RCA Laboratories' Microwave Technology Center, where he designed a cooled low-noise amplifier for a ground-based satellite terminal and a low-noise amplifier for a Ku-band down converter for a geostationary satellite. He is engaged in the design of state-of-the-art microwave low-noise amplifiers and down converters and other advanced microwave components.

Mr. Askew has published several papers on microwave solid-state components, and holds two U.S. patents. He is a member of the IEEE and of its Professional Group on Microwave Theory and Techniques.

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He has written more than 15 papers and technical reports in fields including transmitters, amplifiers, radar systems, high-bit-rate modulator/demodulators, and other microwave and rf topics. Mr. Aubert is a member of Eta Kappa Nu and the IEEE.

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George R. Busacca received a BSEET degree from Trenton State College in 1977 and an MBA degree from Monmouth College in 1983. At RCA Astro-Electronics, which he joined in 1981, he has been designing low-noise microwave amplifiers for communication satellite transponders. As lead engineer on the CLNA program, he is responsible for the electrical design and coordination of the thermal and mechanical design efforts. His designs are in use on the Spacenet C/Ku-band satellites and are also to be employed on Ku-band GSTAR and RCA Satcom K satellites, scheduled to be launched in 1985. Before joining RCA he designed medium- and high-power microwave amplifiers and components from L band through X band at Microwave Semiconductor Corp.

Raymond L. Camisa received the BEE, MEE, and PhD degrees from the City University of New York in 1965, 1969, and 1974, respectively. In 1974, Dr. Camisa joined the Microwave Technology Center at RCA Laboratories. In addition to his research on GaAs field-effect-transistor devices and circuits, he has contributed to the development of the first 1-W, X-band power transistor in 1974. In 1979, he received an RCA Laboratories Outstanding Achievement Award for developing microwave lumped-element GaAs FET amplifiers. In 1983 he was promoted to Senior Member of the Technical Staff. He is leading a team investigating lumped-element broadband FET power amplifiers and millimeter-wave transistors and circuits.

Dr. Camisa holds five U.S. patents and has published more than 20 papers on low-noise parametric amplifiers, microwave integrated circuits, MIS varactors, and GaAs FET amplifiers, oscillators, and devices. He has served on many local and regional IEEE committees and is a founder and past chairman of the Princeton Area Microwave Theory and Techniques and Electron Devices (MTT/ED) Chapter. He also chaired the IEEE Princeton Section and, subsequently, the IEEE Metropolitan Societies Activities Council (METSAC), which coordinates the activities of all IEEE groups in the tri-state area. He is a Director of ELECTRO, the largest electronics technical and marketing show in the East, and was the Convention Director of ELECTRO 83.

Alex Chuchra received a BS degree in Mechanical Engineering from the New Jersey Institute of Technology in 1982. After graduation he was involved in the computer-aided thermodynamic optimization of chemical processes. In 1983 he joined RCA Astro-Electronics, Princeton, NJ, where he is responsible for the design and analysis of a satellite thermal system.

Frank P. Cuomo earned an Associate Applied Science (AAS) degree from Mercer County Community College in 1981 and is working toward a BS degree in Electronics Technology at Trenton State College. In 1981 he joined the Microwave Technology Center at RCA Laboratories, Princeton, NJ, as a Research Technician. Mr. Cuomo has worked on the development of device fabrication techniques for GaAs field-effect transistors and monolithic integrated circuits. More recently he has been involved in the research and development of hybrid couplers for use in K-band amplifiers.

Michael T. Cummings received the BSEE degree from New Jersey Institute of Technology in 1975. Between 1976 and 1977 he worked on p-i-n diode circuits for Vectronics Microwave. From 1977 to 1978 he was engaged in developing evanescent-mode waveguide filters at Frequency Engineering Labs. Mr. Cummings joined the Microwave Technology Center at RCA Laboratories, Princeton, NJ, in 1978 and was promoted to Member, Technical Staff, in 1981. He has been extensively involved in the development of solid-state power amplifiers from C to X band. As part of the team that developed the 8.5-watt amplifier for the RCA Satcom satellites, he shared an RCA Laboratories Outstanding Achievement Award in 1982.

Surjit S. Dhillon received the BSc (engineering) Honors degree from the University of London in 1969 and the MSc (microwaves) degree from University College, London, in 1972. From 1972 to 1974 he worked as a microwave development engineer with Marconi Communication Systems Ltd., England, developing low-noise front ends. From 1974 to 1977 he was employed at EMI Electronics, Ltd., England, developing microwave and electronic hardware for fusing radar systems. From 1977 to 1982 he was responsible for developing solid-state microwave subsystems for satellite communication transponders at Spar Aerospace Ltd., Canada.

Mr. Dhillon joined RCA Astro-Electronics, Princeton, NJ, in 1982 and is a Principal Member of the Technical Staff, responsible for the development of the 17/12-GHz communication receiver. He is a member of the IEEE.

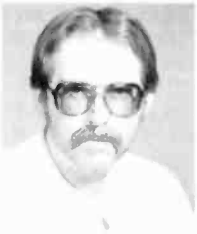
Brian R. Dornan received a BS degree with honors in Electrical Engineering from Newark College of Engineering in 1973, and an MS degree in EE from New Jersey Institute of Technology in 1979. He joined RCA Electronic Components Division in 1968, working on traveling-wave tubes (TWTs) and, in 1972, was promoted to the position of Project Engineer, responsible for the design of voltage-controlled oscillators. In 1977 Mr. Dornan joined the Microwave Technology Center at RCA Laboratories, Princeton, NJ, as a Member, Technical Staff. He is engaged in the development and applications of solid-state microwave devices.

Mr. Dornan was the Lead Design Engineer on the first space-qualified solid-state power amplifier (SSPA) to replace TWTs in commercial satellite applications and, in 1980, received an RCA Laboratories Outstanding Achievement Award for this work. In 1983 he received a David Sarnoff Award for Outstanding Technical Achievement, RCA's highest honor. He has presented and has had published several papers on the design of SSPAs. Mr. Dornan holds a patent for his work on a driver circuit for high-repetition-rate solid-state laser modulation.

Harold B. Goldberg received the BSEE degree from Lafayette College in 1956 and the MSEE degree from Cornell University in 1958. He joined RCA Astro-Electronics, Princeton, NJ, in 1977 and was responsible for designing C-band and K-band communications receivers used in RCA Satcom satellites and other programs. Since 1981 he has been Manager, Receiver Design, with responsibility for all wideband communication receivers and command receivers used on RCA-built communications satellites. Mr. Goldberg is a member of Tau Beta Pi and the IEEE.

Paul A. Goldgeier received the BS degree in Electrical Engineering from the University of Rhode Island in 1981 and expects to complete the MS degree at the Polytechnic Institute of New York in 1985. Since 1981, when he joined RCA Astro-Electronics, he has been involved with microwave receiver design, primarily in the area of low-noise amplifiers. More recently, he has been responsible for the design of 30-GHz LNAs and has been participating in the development of miniature microwave circuits at the RCA David Sarnoff Research Center. Mr. Goldgeier is a member of Tau Beta Pi.

Galina Kelner received the MS degree from Mendeleev Institute of Chemical Technology, Moscow, USSR, in 1956. She immigrated to the United States in 1976. From 1976 to 1980, at the Research Triangle Institute, North Carolina, she was engaged in the growth and characterization of epitaxial III-V materials. In 1980 she joined the Naval Research Laboratory, Washington, DC, where she has been working on GaAs and InP device design and fabrication.



Francis J. McGinty graduated from Pennco Technical Institute in 1978 and received an Associate degree in Electronics Technology from Bucks County College in 1980. From 1974 to 1980 he worked for the Milton Roy Co., originally as a Quality Control Technician in their Flow Control Division. There he received a special commendation for his contribution to dialysate metering-pump technology. In 1978 he transferred to Research and Development as an Engineering Technician to assist in the development of metering pumps and electronic-flow instrumentation.

In 1980 Mr. McGinty joined the Microwave Technology Center at RCA Laboratories, Princeton, NJ, as a Research Technician, to help and develop solid-state power amplifiers. Promoted to Technical Associate in 1983, he has been working on miniature microwave technology.

Shabbir S. Moochalla received a BS degree with distinction in Electronics Engineering in 1973 in India and an MS degree in Electrical Engineering in 1977 from the State University of New York at Buffalo. He worked for Defence Research Lab in India on ferrite components. After receiving the MSEE degree, he joined Microwave Semiconductor Corp. to work on broadband circuit design, internally matched devices, and overlay bipolar transistor processing.

Mr. Moochalla joined RCA Astro-Electronics, Princeton, NJ, as a Senior Member, Technical Staff, in 1981. He is involved in developing broadband 20-GHz amplifiers and K-band amplifiers, and is the lead engineer for the driver/ALC amplifier for the DBS program. He has published several papers in his fields of interest.

Robert E. Neidert received the BE(EE) degree from Vanderbilt University in 1959 and has done graduate work at the University of Florida, St. Petersburg. From 1959 to 1962, at Sperry Microwave Electronics Company, he was engaged in developing microwave components for radar systems. From 1962 to 1969, as Senior Design Engineer and Project Leader at the General Electric Co., Communications Products Department, he was responsible for the design and development of microwave components and solid-state sources for TV and multiplex telephony radio relay equipment. From 1969 to 1972 he was a Principal Engineer at Radiation Systems, Inc., working on antenna and antenna feed network design.

In 1972 he joined the Naval Research Laboratory, Washington, DC, and has since been involved in research on microwave circuits for solid-state devices and on monolithic microwave and millimeter-wave devices and circuits. He has written numerous papers in the fields of communications systems components, microwave integrated circuits, computer-aided microwave circuit design, bipolar and FET amplifier design, and FET modeling. Mr. Neidert is a member of Tau Beta Pi.

Markus Nowogrodzki was graduated with the degrees of Bachelor of Electrical Engineering, cum laude, in 1948, and Master of Electrical Engineering, in 1951, both from the Polytechnic Institute of New York. From 1948 until 1951, he was a Microwaves Engineer at Hazeltine Corp., working on microwave cavities and test procedures for IFF systems. From 1951 until 1955, he was with Amperex Electronic Corp., where he helped establish the magnetron development department and rose to the position of Supervising Engineer, Magnetron Development. In 1955, he joined RCA Electronic Components, engaged in the development and manufacturing of magnetrons, microwave triodes, traveling-wave tubes, and solid-state subsystems. As Manager, Traveling-Wave Tube Operations, he supervised a department comprising design, manufacturing, applications, and program-control activities.

During 1967–73, Mr. Nowogrodzki worked in microwave tube and product management at North American Philips and Polyflon Corporation. In 1973, he rejoined RCA as Manager, Division Liaison, at the Microwave Technology Center (MTC), RCA Laboratories, Princeton, NJ. He is now in charge of MTC's Subsystems and Special Projects group. Mr. Nowogrodzki holds six U.S. patents and has written more than 20 papers on various aspects of microwave component design and applications. He is a member of the New York Academy of Sciences, Eta Kappa Nu, and Tau Beta Pi, and a Senior member of the IEEE.

Michael J. Noyes joined Marconi Space and Defense Systems in 1975 and attended Technical University as a sponsored student until 1983. While working as a mechanical engineer in the microwave group at Marconi, he developed a strong microwave background, designing components at 35, 60, and 94 GHz including filters, Gunn VCOs, and p-i-n switches. He joined RCA Astro-Electronics in 1984 as a Member of the Antenna Microwave Mechanical group and has produced component and waveguide antenna designs for the Satcom Ku and DBS satellite programs.

Walter F. Reichert graduated from DeWitt Clinton High School in 1952 and served in the U.S. Army from 1954 to 1956. From RCA Institutes he received a certificate for completing the General Electronics Technology course in 1961. Mr. Reichert then attended Rutgers University and later Middlesex County College, receiving an Associate degree in Electrical Engineering from MCC in 1971. He joined RCA Laboratories, Princeton, NJ, as a Research Technician in 1961 and participated in experiments dealing with cesium recombination, double-stream amplifiers, crystals acoustics, surface wave propagation in CdS, and GaAs Schottky-barrier diodes. He also worked on the development of polyimides for use as a dielectric on integrated circuits and with active semiconductor devices.

Mr. Reichert was promoted to Technical Staff Associate in 1973, and to Associate Member of the Technical Staff in 1978. For his contributions to the development of GaAs power field-effect transistors (FETs) he shared an RCA Laboratories Outstanding Achievement Award in 1976. He is still involved in developing GaAs transistors. Mr. Reichert holds eight U.S. patents.

Arye Rosen received the BSEE degree cum laude from Howard University in 1963 and the MScE degree from Johns Hopkins University (which he attended on a Gillman Fellowship) in 1965. He was an instructor at Johns Hopkins during 1963–64. From then until 1967, Mr. Rosen was concerned with systems design at General Telephone and Electronics International, Inc., and American Electronics Laboratories, Inc. In 1967, he joined RCA Laboratories, Princeton, NJ, as a Member of the Technical Staff in the Microwave Technology group. Mr. Rosen is responsible for the research and development of millimeter-wave devices and circuits, as well as rf silicon devices, such as p-i-n and varactor, and was extensively involved in the thermal studies of those devices. His work on integrated diode arrays paved the way for chips power combining in microwave and millimeter waves. He shared a 1972 RCA Laboratories Outstanding Achievement Award for the development of S-band TRAPATT amplifiers and, in 1982, received an individual RCA Laboratories Outstanding Achievement Award for developing high-performance silicon p-i-n diodes for application to communications systems.

From 1970 to 1971, on leave of absence from RCA, Mr. Rosen engaged in research (on a departmental Fellowship) in the Division of Cardiology at Jefferson Medical College in Philadelphia. There he received the degree of MSc in Physiology and later was appointed an Associate in Medicine. He now holds an appointment of Adjunct Professor at Drexel University, in the Department of Electrical and Computer Engineering.

Mr. Rosen is the author of more than 40 technical papers and presentations and holds 21 patents in the microwave field. He is a member of Tau Beta Pi, Sigma Xi, and the Association of Professional Engineers of British Columbia (Canada), as well as a Senior member of the IEEE. He has been included in *Who's Who in Technology Today*. Mr. Rosen is also a member of the Physiological Society, Philadelphia.

Paul J. Stabile received the BEEE degree summa cum laude from Manhattan College in 1979 and the MSEE degree from Rutgers University in 1982. In 1979 he joined the RCA Engineering Rotation program. His assignments included microwave amplifier design, digital circuit development, and computer-aided design techniques for VLSI circuitry. Later that year, he joined the Microwave Technology Center at RCA Laboratories, Princeton, NJ.

Mr. Stabile has been engaged in the research and development of microwave and millimeter-wave devices and circuits, including millimeter-wave IMPATT diodes, oscillators and amplifiers, high-power p-i-n diodes, frequency multipliers, and phase shifters. More recently, as a Member of the Technical Staff, he has been working on silicon millimeter-wave integrated circuits. He has written more than a dozen technical papers and has one U.S. patent pending. Mr. Stabile is a member of Epsilon Sigma Pi of Manhattan College, Etta Kappa Nu, Tau Beta Pi, and the IEEE.

Gordon C. Taylor received the BS, MS, and PhD degrees in Electrical Engineering in 1969, 1972, and 1976 from Rutgers University. His PhD thesis was on switching and conduction mechanisms of polycrystalline thin films of TiO_2. From 1976 to 1977 he was employed by the Electronic Technology Division of the National Bureau of Standards. There he engaged in the design of test structures and test patterns for integrated-circuit process monitoring and analysis.

In 1977 Dr. Taylor joined the Microwave Technology Center at RCA Laboratories, Princeton, NJ, as a Member of the Technical Staff. Since then he has been working on the development of device fabrication technology for GaAs field-effect transistors. He holds one U.S. patent on GaAs device processing. Dr. Taylor has authored or coauthored several papers and has given presentations on the fabrication technology of discrete GaAs FETs and of monolithic integrated circuits on GaAs substrates. He is a member of Tau Beta Pi, Eta Kappa Nu, the IEEE, and the American Vacuum Society.

Glenn R. Thoren received the BS degree in Applied and Engineering Physics from Cornell University in 1972, and the MS degree in Applied and Engineering Physics from Cornell University, in 1973. He has also received the PhD degree in Electrical Engineering from Cornell University in 1980, while sponsored by a Raytheon Company Fellowship.

Dr. Thoren has been with Raytheon since 1971 and with the Missile Microwave and Antenna Department of the Missile Guidance Laboratory and the Antenna/Microwave Department of the Radar Systems Laboratory since 1973. He has directed millimeter-wave technology and development programs as Manager of the Millimeter Wave Transmitters and Systems Section of the Antenna/Microwave Department, and is currently on the Technical Staff of the Radar Systems Laboratory responsible for new efforts in millimeter-wave systems. He has designed, developed, and supervised research on many state-of-the-art IMPATT diode power combiners for active seeker missiles and projectiles from *X*-band through *W*-band. He completed development work on surface acoustic-wave delay lines for the PATRIOT air defense system in 1973–74. He has characterized and analyzed both silicon and GaAs IMPATTs up to 100 GHz. He discovered the delayed secondary avalanche (DSA) phenomena in millimeter-wave IMPATTs during his PhD studies at Cornell. Dr. Thoren holds four patents for advanced solid-state power combiners circuits and has published and presented more than 25 papers on solid-state power sources and millimeter-wave technology.

Dr. Thoren has been actively involved in IEEE activities for many years. He is a past Chairman (1982–83) and Vice Chairman (1981–82) of the New England Council Chapter of the Microwave Theory and Techniques Society. He has served as Membership Development Subcommittee Chairman for the International MTT-S ADCOM (1974–80). He has also served as Membership Development Chairman for Division IV (1981–83). He was Co-Chairman of the 1983 MTT-S Symposium Publications Committee that produces the Symposium Digest, and a member of both the Technical Program Committee and the Symposium Steering Committee. He was a member of the Technical Program Committee for Electro '84 and is currently serving as a member of the Executive Committee of the Boston Section. He is also a member of the MTT and ED Societies, as

well as Eta Kappa Nu. For Raytheon, he is currently the Chairman of the Raytheon-Cornell University College Relations Committee and the Technology Leader for Millimeter Wave Development at Bedford Laboratories. He was named Engineer of the Month in October 1982 for the development of a versatile *W*-band IMPATT power combiner.

L. Chainulu Upadhyayula received the BSc degree in Physics and the MSc in Applied Physics from Andhra University, India, in 1955 and 1958, respectively, and the PhD degree in Engineering from Brown University in 1968. During 1968–69 Dr. Upadhyayula was a Post Doctoral Fellow in Engineering at Brown, studying tunneling through superconducting metal-insulator-metal structures at cryogenic temperatures.

In 1969, Dr. Upadhyayula joined the Microwave Technology Center at RCA Laboratories, Princeton, NJ, as a Member of the Technical Staff. His work at RCA includes 4- to 16-GHz GaAs transferred-electron (Gunn) amplifiers (TEAs), high-efficiency IMPATTs, 18- to 40-GHz InP oscillators and amplifiers, transferred-electron logic devices (TELDs), GaAs field-effect transistors (FETs), GaInAs insulated-gate FETs, and high-speed logic circuits. He is engaged in developing GaAs MESFET and GaInAs MISFET technologies for MSI and LSI logic circuits working at clock rates above 1–2 GHz. The logic circuits under development are gigabit-sampling rate analog-to-digital converters (ADCs), programmable dividers, and pseudorandom code generators.

Dr. Upadhyayula has published several technical papers in these areas. He was awarded a General Telephone and Electronics Fellowship in 1967–68 for his graduate study. In 1970, he shared an RCA Laboratories Outstanding Achievement Award for the development of GaAs transferred-electron amplifiers. He holds 14 U.S. patents and has several disclosures pending. Dr. Upadhyayula is a Senior member of the IEEE and a member of Sigma Xi. He is very active in the IEEE activities at the local as well as national level and is a past vice-chairman and chairman of the ED/MTT Chapter, Princeton Section. Since 1983 he has been serving on the Digital Microwave Systems Committee (MTTS-9) of the Microwave Theory and Techniques Society.

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Ralph F. Ciafone, Editor